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Technical Memorandum No. 33-127

Science Subsystem Operations, Ranger Follow-On

R. P. Del Negro

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA

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National Aeronautics & Space Administration

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FIGURES (Cont'd)

NOTE

A decision was reached in the early part of 1963 to exclude all scientific experiments from the *Ranger* Follow-On spacecraft except the television system. This report describes some equipment and operations techniques common to many of the *Ranger* Follow-On spacecraft series, together with details of the equipment developed for a particular series —*Rangers* 7–9.

ABSTRACT

A brief description of the *Ranger* Follow-On scientific mission is given. Scientific experiments originally aboard the *Ranger* Follow-On spacecraft are discussed in some detail. GSE components and testing capabilities are described.

I. INTRODUCTION

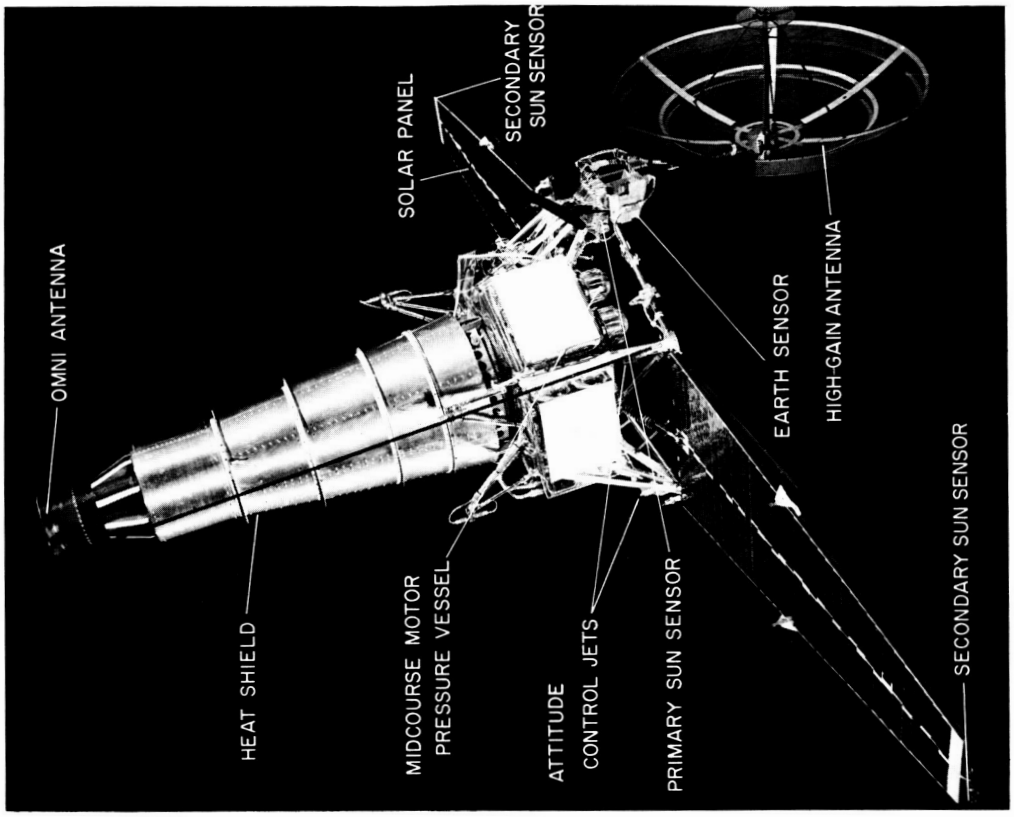
The *Ranger* Follow-On spacecraft have been designed to accomplish two scientific objectives:

1. To acquire knowledge of lunar topography sufficient for determination of its gross effects on lunar landing vehicles. This objective will be achieved by the *Ranger* television system.
2. To acquire knowledge of the fields and particles environment of cislunar and lunar space which may be of importance to manned lunar flights. This objective will be achieved through the use of fields and particles experiments.

The basic spacecraft bus developed on the *Ranger 1* through *5* series will be utilized as the supporting spacecraft structure after minimum modifications are made for mechanical compatibility. The scientific experiments to be flown on the *Ranger* Follow-On spacecraft were:

1. Cosmic dust detectors
2. Low-energy plasma probe
3. Electron flux detector
4. Electron-proton spectrometer
5. Ion chamber
6. Particle flux detector
7. Search coil magnetometer
8. Low-energy ion detector

All experiments were to provide data from the time of the *Agena B* separation to lunar impact except during the midcourse maneuver. The experiments would be receptive to various types of information such as micrometeorite impacts (cosmic dust detector) and fluctuating magnetic fields (search coil magnetometer). A brief explanation of the function of each experiment is presented in this report. Figure 1 shows the *Ranger* spacecraft; Fig. 2 is a composite drawing of the *Ranger* vehicle and spacecraft.



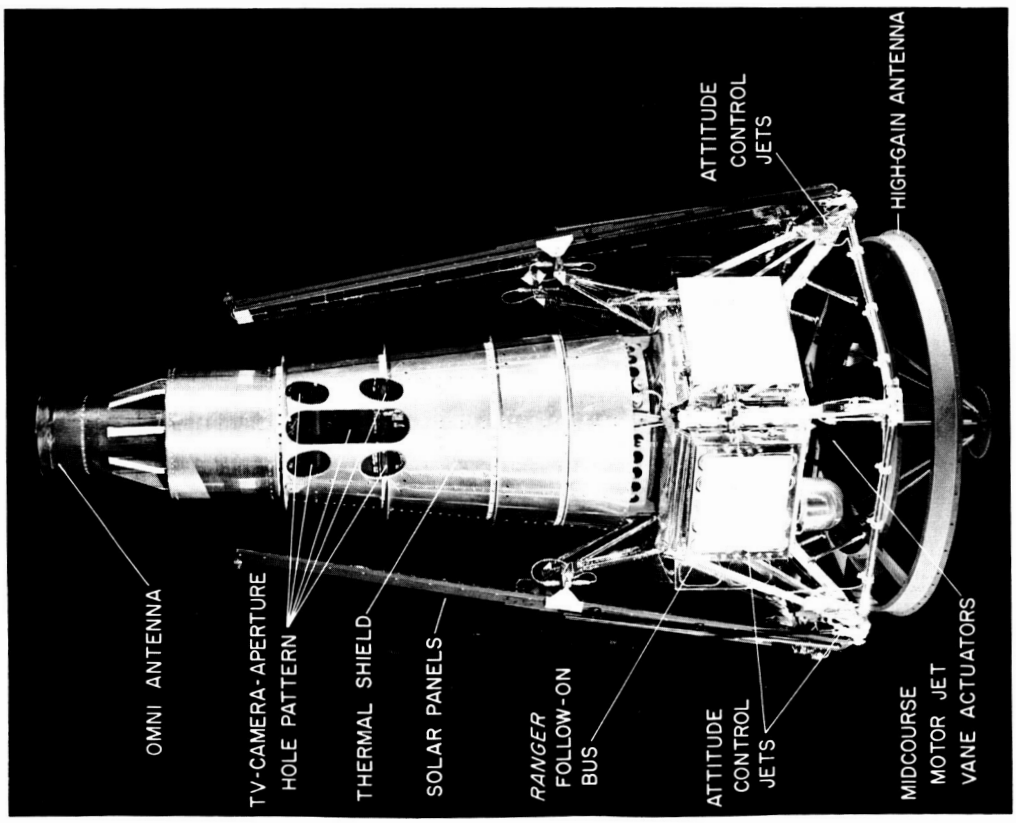


Fig. 1. *Ranger* Follow-On spacecraft

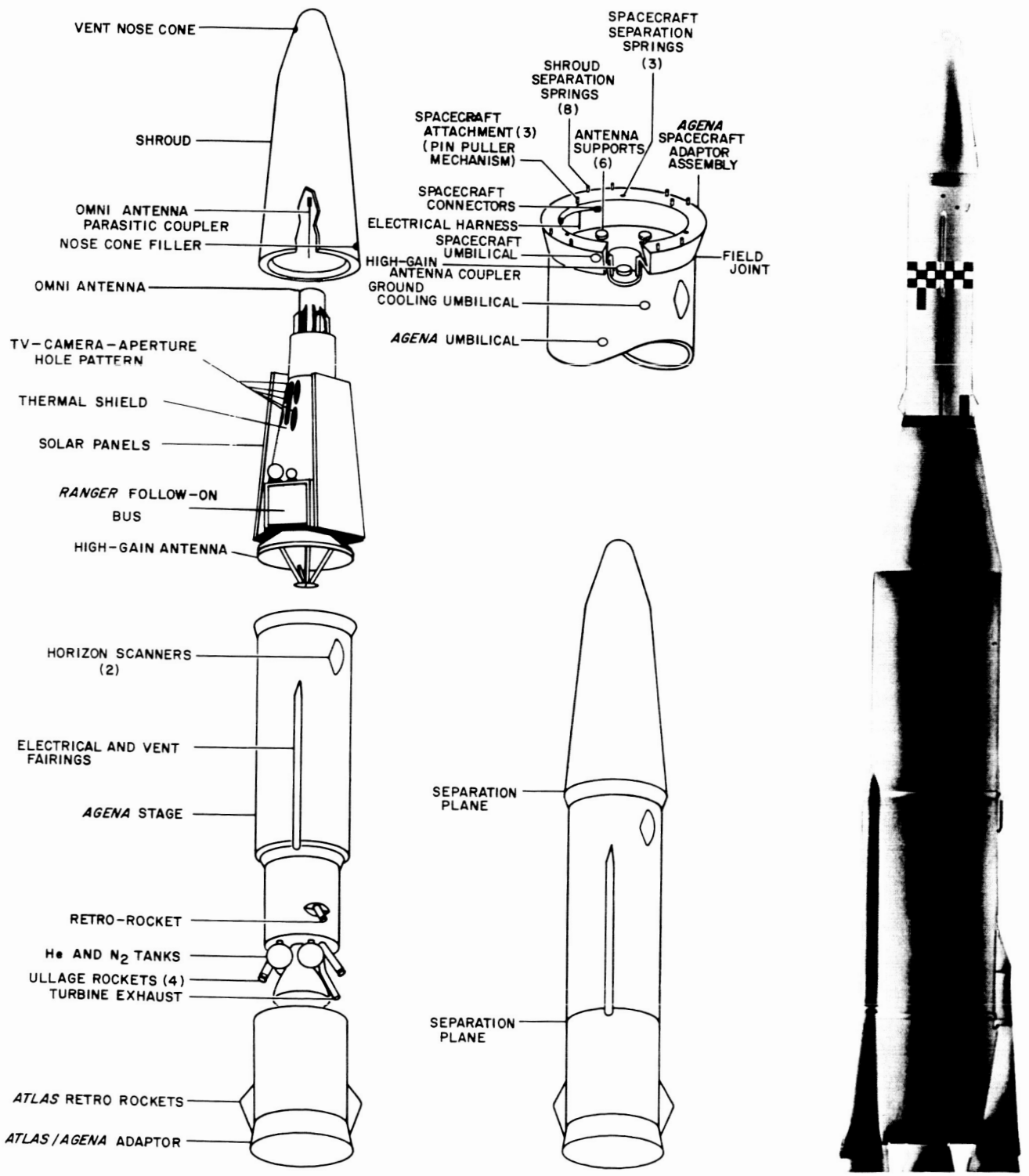


Fig. 2. *Ranger* Follow-On vehicle and spacecraft

II. SYSTEM OPERATION

The purpose of this section is to familiarize personnel with the system operation of the *Ranger* Follow-On scientific package. Discussion of system functions is broken down into three subsections: Data flow, power distribution, and interconnecting cabling (which includes wiring and test cabling).

A. Data Flow

The scientific data from the experiments are in three forms: analog, digital, and binary. In addition, the instruments are calibrated and preliminary processing of the data is performed on the spacecraft prior to being telemetered to Earth. A data sequencing and handling system called the data automation system (DAS) has been developed which performs these functions. Specifically, these are analog-to-digital conversion, digital-to-digital conversion, sampling timing, and sequencing commands.

The transformed data are loaded into an 8-stage counter shift register which is the heart of the data handling section of the DAS. This register acts as a counter for analog-to-digital conversion, a pseudonoise generator for subframing and framing the data, and a buffer storage for the digital-to-digital conversion. The information contained in the 8-stage register is then transferred to spacecraft telemetry for relay to the ground communication on Earth.

Approximately 24 min after the spacecraft is launched from Earth, the second stage of the *Agena B* is separated from the spacecraft and science power is turned on. Scientific information from the DAS is then sent back to Earth on telemetry channel 6. Approximately 16 hr after launch, science power is turned off and the spacecraft is commanded into its midcourse maneuver mode. During this mode telemetry channel 6 is used for midcourse information. Upon completion of the midcourse maneuver, the spacecraft goes into a cruise mode, and the central computer and sequencer (CC and S) turns on both science power and the TV subsystem engineering telemetry channel 8. Approximately 55 min before lunar impact, the terminal maneuver is initiated. The TV subsystem warmup power is applied 15 min before impact, and the full power to the entire subsystem is applied 10 min before lunar impact. Near lunar impact, TV information is telemetered back to Earth by two TV transmitters. Scientific and TV data are transmitted in real time from the spacecraft to Earth until lunar impact.

Extensive data processing and computer capability will be available at the central computer facility of the Jet Propulsion Laboratory. Frequency-modulated data from the spacecraft are received at a DSIF station and recorded on magnetic tape. The magnetic tape is then sent to the JPL telemetry processing station, where the signal is demodulated and put into the proper format for recording on the Ampex FR400 digital tape deck. All of the individual tapes from the Ampex FR400 are placed in chronological order and recorded on one magnetic tape for the IBM 7090 computer analysis. Data are then displayed by the IBM 7090 computer in decimal line format for the cognizant engineers and scientists. Figure 3 is a block diagram of the telemetry data flow.

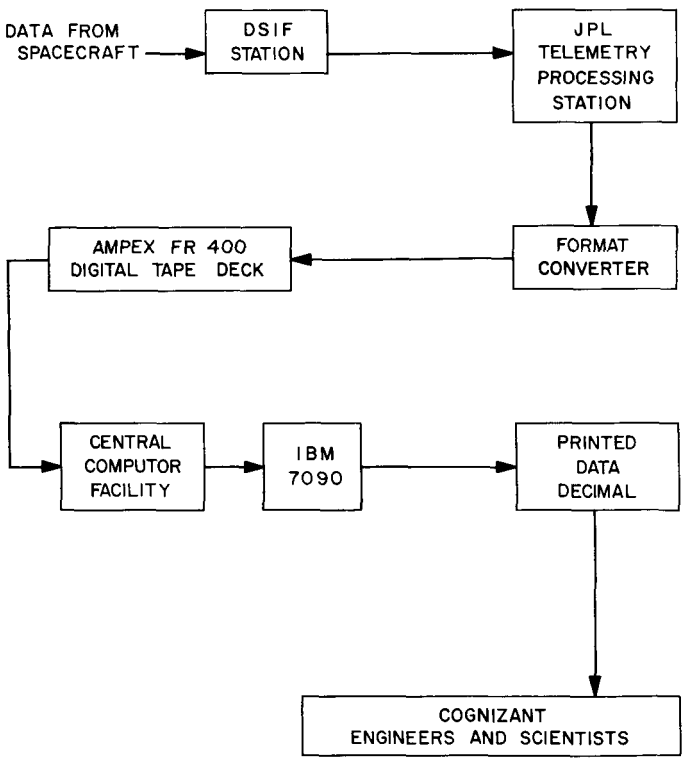


Fig. 3. Telemetry data flow block diagram

B. Power Distribution

All the scientific instruments receive power from the primary spacecraft power supply. The inverter operates from +31.5- and −9-vdc power supplied from the spacecraft power source and a 4800-cps sync signal turned on by CC and S.

At T +24 min, science power is turned on by CC and S, and the inverter sends 52-v, 2400-cps power to the science transformer-rectifier (TR) unit. The science TR unit in turn supplies two outputs: a regulated 28 vdc to the low-energy plasma, low-energy ion, and electron-proton spectrometer experiments, and 52-v, 2400-cps to the DAS, search coil magnetometer, electron flux detector, particle flux detector, and cosmic dust detector experiments. The experiments which receive the 2400-cps power rectify this voltage to meet specific needs as described in the experiment sections.

C. *Interconnecting and Test Cabling*

Figure 4 is the science subsystem block diagram. Figure 5 is a cabling master block diagram for a systems test configuration. Figure 6 shows the science interconnecting cables and functions.

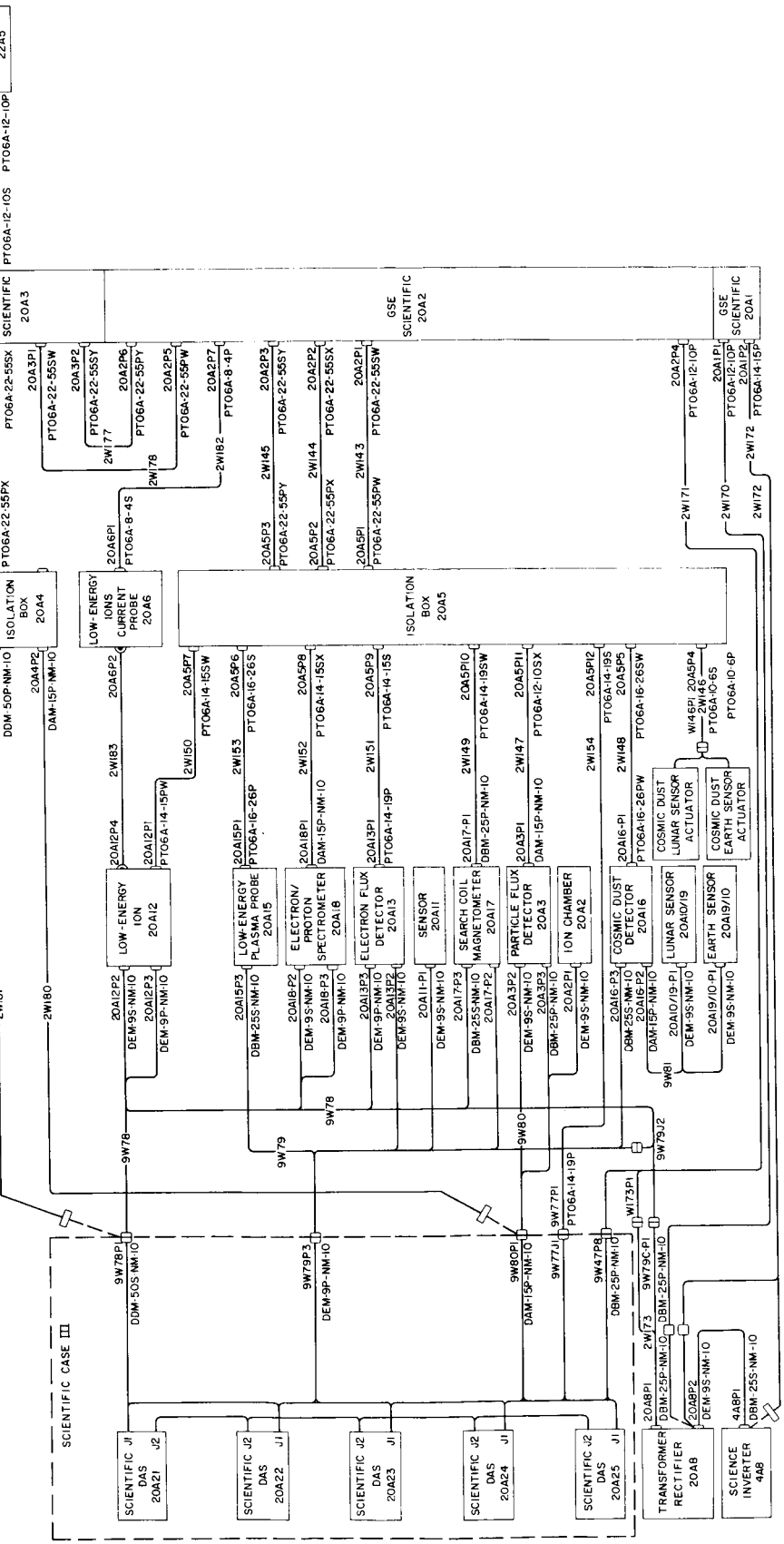
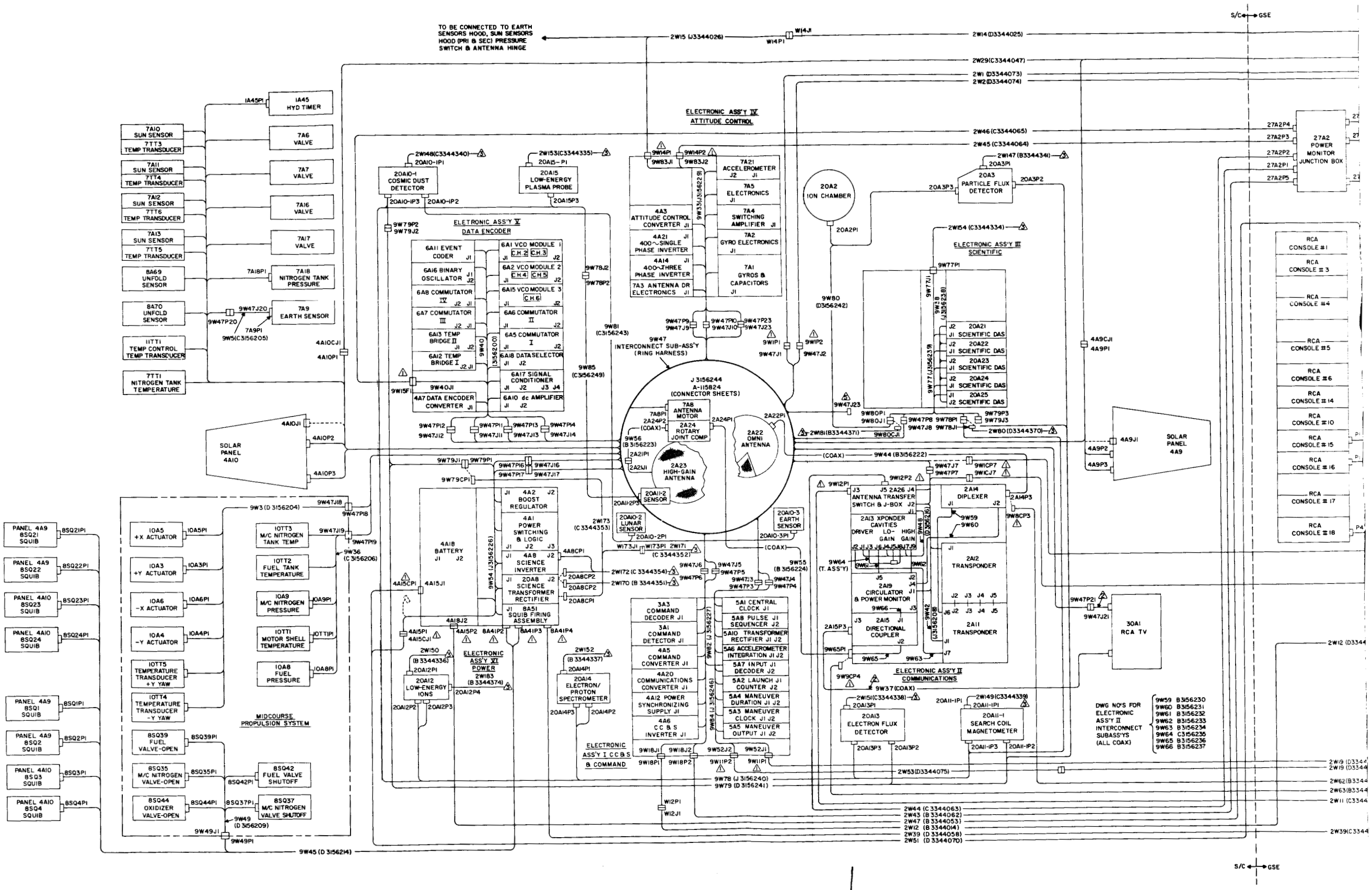


Fig. 4. Science subsystem cabling block diagram


TO BE CONNECTED TO EARTH SENSORS HOOD, SUN SENSORS HOOD (PRI & SEC) PRESSURE SWITCH & ANTENNA HINGE
2WI5 (J3344026)
W14J1
W14P1
2WI4(D3344025)
S/C
GSE
2W29(C3344047)
2WI (D3344073)
2W2(D3344074)
ELECTRONIC ASS'Y IV
ATTITUDE CONTROL
2W46(C3344065)
2W45 (C3344064)
1A45P1
1A45 HYD TIMER
7A10 SUN SENSOR
7TT3 TEMP TRANSDUCER
7A6 VALVE
7A11 SUN SENSOR
7TT4 TEMP TRANSDUCER
7A7 VALVE
7A12 SUN SENSOR
7TT6 TEMP TRANSDUCER
7A16 VALVE
7A13 SUN SENSOR
7TT5 TEMP TRANSDUCER
7A17 VALVE
8A69 UNFOLD SENSOR
7A18P1
7A18 NITROGEN TANK PRESSURE
8A70 UNFOLD SENSOR
9W47J20
9W47P20
7A9P1
7A9 EARTH SENSOR
9W5(C3156205)
11TT1 TEMP CONTROL TEMP TRANSDUCER
4A10CJ1
4A10P1
7TT1 NITROGEN TANK TEMPERATURE
2WI48(C3344340)
20A10-1P1
20A10-1 COSMIC DUST DETECTOR
20A10-1P3
20A10-1P2
9W79P2
9W79J2
2WI53(C3344335)
20A15-P1
20A15 LOW-ENERGY PLASMA PROBE
20A15P3
ELETRONIC ASS'Y V
DATA ENCODER
6A11 EVENT CODER J1
6A16 BINARY OSCILLATOR J1 J2
6A8 COMMUTATOR IV J2 J1
6A7 COMMUTATOR III J2 J1
6A13 TEMP BRIDGE II J1 J2
6A12 TEMP BRIDGE I J2 J1
6A1 VCO MODULE 1 CH.2 CH.3 J1 J2
6A2 VCO MODULE 2 CH.4 CH.5 J1 J2
6A15 VCO MODULE 3 CH.6 J1 J2
6A6 COMMUTATOR II J1 J2
6A5 COMMUTATOR I J1 J2
6A18 DATA SELECTOR J1 J2
6A17 SIGNAL CONDITIONER J1 J2 J3 J4
6A10 dc AMPLIFIER J1 J2
9W40 (J3156200)
9W40J1
9W15F
4A7 DATA ENCODER CONVERTER J1
9W78J2
9W78P2
9W85 (C3156249)
9W14P1
9W14P2
9W83J1
9W83J2
9W33(J3156228)
7A21 ACCELEROMETER J2 J1
7A5 ELECTRONICS J1
7A4 SWITCHING AMPLIFIER J1
7A2 GYRO ELECTRONICS J1
7A1 GYROS & CAPACITORS J1
4A3 ATTITUDE CONTROL CONVERTER J1
4A21 400~SINGLE PHASE INVERTER J1
4A14 400~THREE PHASE INVERTER J1
7A3 ANTENNA DR ELECTRONICS J1
9W81 (C3156243)
9W47P9
9W47J9
9W47P10
9W47J10
9W47P23
9W47J23
9W1P1
9W47J1
9W1P2
9W47J2
9W47
INTERCONNECT SUB-ASS'Y (RING HARNESS)
J3156244 A-115824 (CONNECTOR SHEETS)
7A8P1
2A24P2 (COAX)
7A8 ANTENNA MOTOR
2A24 ROTARY JOINT COMP
2A24P1
2A22P1
2A22 OMNI ANTENNA
2A23 HIGH-GAIN ANTENNA
2A2P1
2A2J1
9W56 (B3156223)
20A2 ION CHAMBER
20A2P1
9W80 (D3156242)
20A3P1
20A3 PARTICLE FLUX DETECTOR
20A3P3
20A3P2
2WI54 (C3344334)
ELECTRONIC ASS'Y III
SCIENTIFIC
9W77P1
9W77J1
9W18 (J3156238)
J2 20A21 J1 SCIENTIFIC DAS
J2 20A22 J1 SCIENTIFIC DAS
J2 20A23 J1 SCIENTIFIC DAS
J2 20A24 J1 SCIENTIFIC DAS
J1 20A25 J2 SCIENTIFIC DAS
9W77 (J3156239)
9W47J23
9W80P1
9W80J1
9W80J2
9W78P1
9W78J1
9W79P3
9W79J3
2WI80(D3344370)
2WI81(B3344371)
4A9CJ1
4A9P1
4A9P2
4A9P3
SOLAR PANEL 4A9
4A10J1
4A10P2
4A10P3
SOLAR PANEL 4A10
9W44 (B3156222)
9W47J7
9W47P7
9W1CP7
9W1CJ7
9W79J1
9W79P1
9W47P16
9W47J16
9W47P17
9W47J17
9W79CP1
2A1I-2 SENSOR
20A1I-2P3
20A10-2 LUNAR SENSOR
20A10-2P1
20A10-3 EARTH SENSOR
20A10-3P1
9W12P1
9W12P2
J3 J5 2A26 J4 ANTENNA TRANSFER SWITCH & J-BOX J2 J1
2A14 DIPLEXER J1 J2
2A14P3
9W8CP3
2A13 XPONDER CAVITIES DRIVER LO- HIGH GAIN GAIN
9W59
9W60
2A12 TRANSPONDER
2A19 CIRCULATOR & POWER MONITOR
2A15 DIRECTIONAL COUPLER
9W64 (T. ASS'Y)
9W61
9W62
9W66
9W65
9W65P1
9W63
2A15P3
9W9CP4
ELECTRONIC ASS'Y II
COMMUNICATIONS
9W37 (COAX)
2WI51(C3344338)
20A13P1
20A13 ELECTRON FLUX DETECTOR
20A13P3
20A13P2
2WI49(C3344339)
20A11-1P1
20A11-1 SEARCH COIL MAGNETOMETER
20A11-1P3
20A11-1P2
9W47P21
9W47J21
30A1 RCA TV
27A2P4
27A2P3
27A2P2
27A2P1
27A2P5
27A2 POWER MONITOR JUNCTION BOX
RCA CONSOLE #1
RCA CONSOLE #3
RCA CONSOLE #4
RCA CONSOLE #5
RCA CONSOLE #6
RCA CONSOLE #14
RCA CONSOLE #10
RCA CONSOLE #15
RCA CONSOLE #16
RCA CONSOLE #17
RCA CONSOLE #18
DWG NO'S FOR ELECTRONIC ASS'Y II INTERCONNECT SUBASS'YS (ALL COAX)
9W59 B3156230
9W60 B3156231
9W61 B3156232
9W62 B3156233
9W63 B3156234
9W64 C3156235
9W65 B3156236
9W66 B3156237
4A18 BATTERY J1 J2
9W54 (J3156226)
4A1 POWER SWITCHING & LOGIC J1 J2 J3
4A2 BOOST REGULATOR J1 J2
4A8 SCIENCE INVERTER J1 J2
20A8 SCIENCE TRANSFORMER RECTIFIER J1 J2
8A51 SQUIB FIRING ASSEMBLY J1
4A8CP1
20A8CP2
20A8CP1
4A8J2
4A8P1
4A8P2
4A8P3
4A8P4
4A15P1
4A15CJ1
4A15J1
4A15P2
8A41P2
8A41P3
8A41P4
2WI73 (C3344353)
WI73J1
WI73P1
2WI71 (C 3344352)
2WI72 (C 3344354)
2WI70 (B 3344351)
9W47J6
9W47P6
9W47J5
9W47P5
9W47J3
9W47P3
9W47J4
9W47P4
9W55 (B 3156224)
3A3 COMMAND DECODER J1
3A1 COMMAND DETECTOR J1
4A5 COMMAND CONVERTER J1
4A20 COMMUNICATIONS CONVERTER J1
4A12 POWER SYNCHRONIZING SUPPLY J1
4A6 CC & S INVERTER J1
9W82 (J3156227)
9W84 (J3156246)
5A1 CENTRAL CLOCK J1
5A8 PULSE J1 SEQUENCER J2
5A10 TRANSFORMER RECTIFIER J1 J2
5A6 ACCELEROMETER INTEGRATION J1 J2
5A7 INPUT J1 DECODER J2
5A2 LAUNCH J1 COUNTER J2
5A4 MANEUVER DURATION J1 J2
5A3 MANEUVER CLOCK J1 J2
5A5 MANEUVER OUTPUT J1 J2
9W18J1
9W18J2
9W18P1
9W18P2
9W52J2
9W52J1
9W11P2
9W11P1
ELECTRONIC ASS'Y I C C & S & COMMAND
2WI52 (B 3344337)
20A14P1
20A14 ELECTRON/ PROTON SPECTROMETER
20A14P3
20A14P2
2WI50 (B 3344336)
20A12P1
20A12 LOW-ENERGY IONS
20A12P2
20A12P3
ELECTRONIC ASS'Y VI POWER
2WI63 (B 3344374)
20A12P4
9W3 (D 3156204)
9W47J18
9W47P18
9W47P19
9W47J19
9W36 (C 3156206)
10A5 +X ACTUATOR
10A5P1
10A3 +Y ACTUATOR
10A3P1
10A6 -X ACTUATOR
10A6P1
10A4 -Y ACTUATOR
10A4P1
10TT5 TEMPERATURE TRANSDUCER +Y YAW
10TT4 TEMPERATURE TRANSDUCER -Y YAW
10TT3 M/C NITROGEN TANK TEMP
10TT2 FUEL TANK TEMPERATURE
10A9 M/C NITROGEN PRESSURE
10A9P1
10TT1 MOTOR SHELL TEMPERATURE
10TT1P1
10A8 FUEL PRESSURE
10A8P1
MIDCOURSE PROPULSION SYSTEM
8SQ39 FUEL VALVE-OPEN
8SQ39P1
8SQ35 M/C NITROGEN VALVE-OPEN
8SQ35P1
8SQ42 FUEL VALVE SHUTOFF
8SQ42P1
8SQ44 OXIDIZER VALVE-OPEN
8SQ44P1
8SQ37P1
8SQ37 M/C NITROGEN VALVE SHUTOFF
9W49 (D 3156209)
9W49J1
9W49P1
9W45 (D 3156214)
PANEL 4A9 8SQ21 SQUIB
8SQ21P1
PANEL 4A9 8SQ22 SQUIB
8SQ22P1
PANEL 4A10 8SQ23 SQUIB
8SQ23P1
PANEL 4A10 8SQ24 SQUIB
8SQ24P1
PANEL 4A9 8SQ1 SQUIB
8SQ1P1
PANEL 4A9 8SQ2 SQUIB
8SQ2P1
PANEL 4A10 8SQ3 SQUIB
8SQ3P1
PANEL 4A10 8SQ4 SQUIB
8SQ4P1
2WI9 (D3344
2WI9 (D3344
2W62(B3344
2W63(B3344
2WII (C3344
2W39(C3344
2W44 (C 3344063)
2W43 (B 3344062)
2W47 (B 3344053)
2WI2 (B 3344014)
2W39 (D 3344058)
2W51 (D 3344070)
2WI2 (D3344
2W53(D3344075)
2W78 (J 3156240)
2W79 (D 3156241)
WI2P1
WI2J1
S/C
GSE

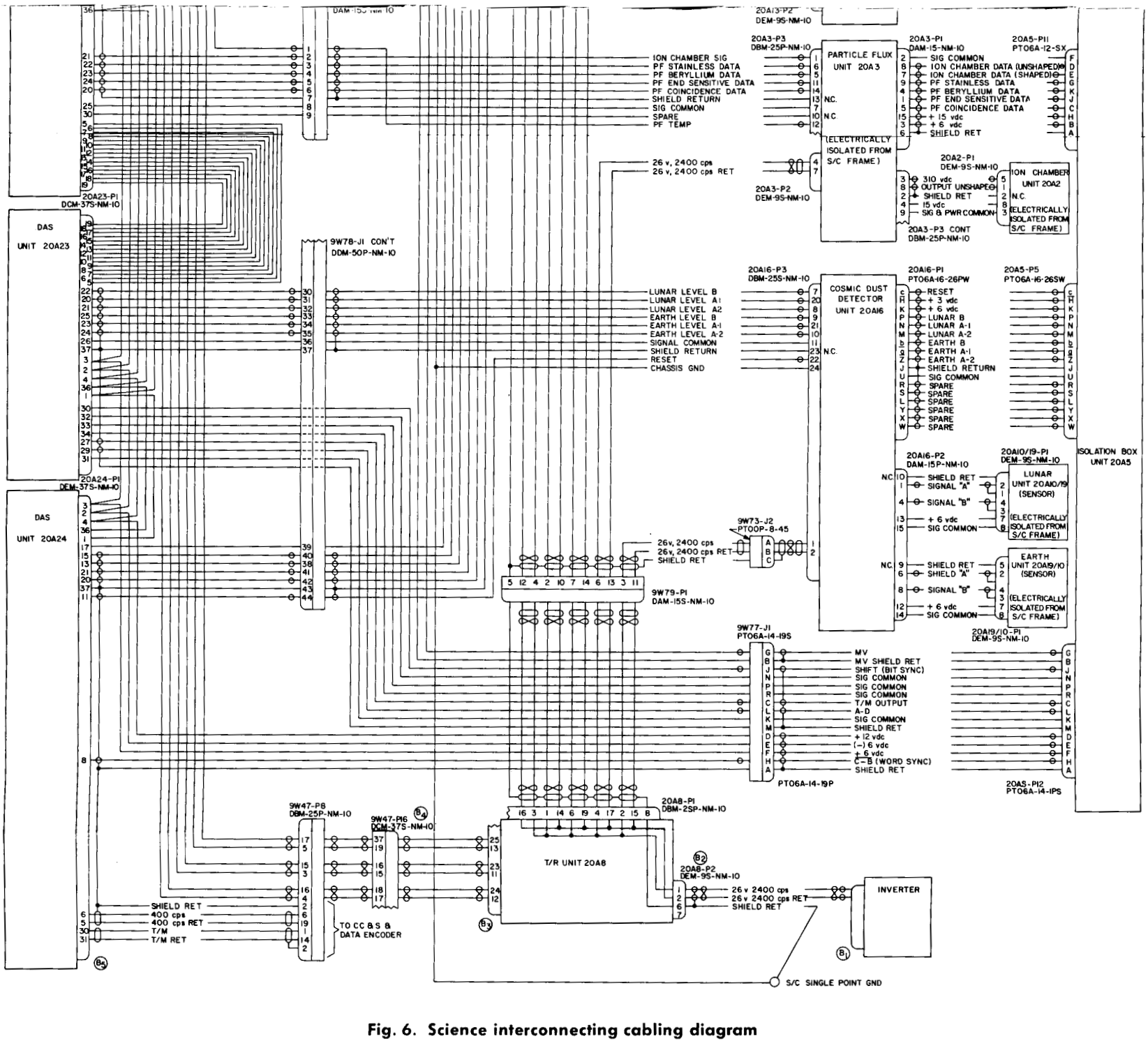


Fig. 6. Science interconnecting cabling diagram

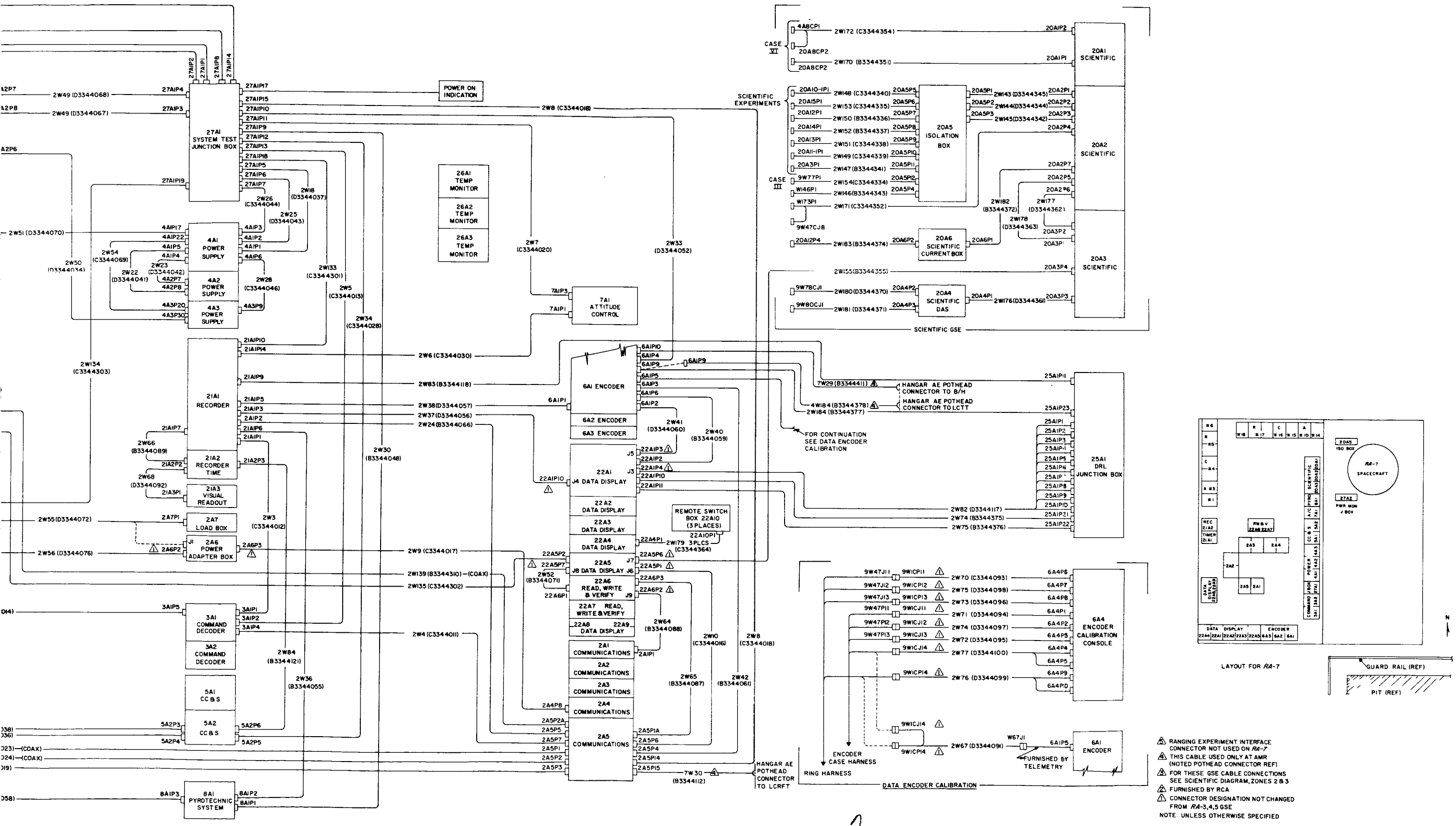
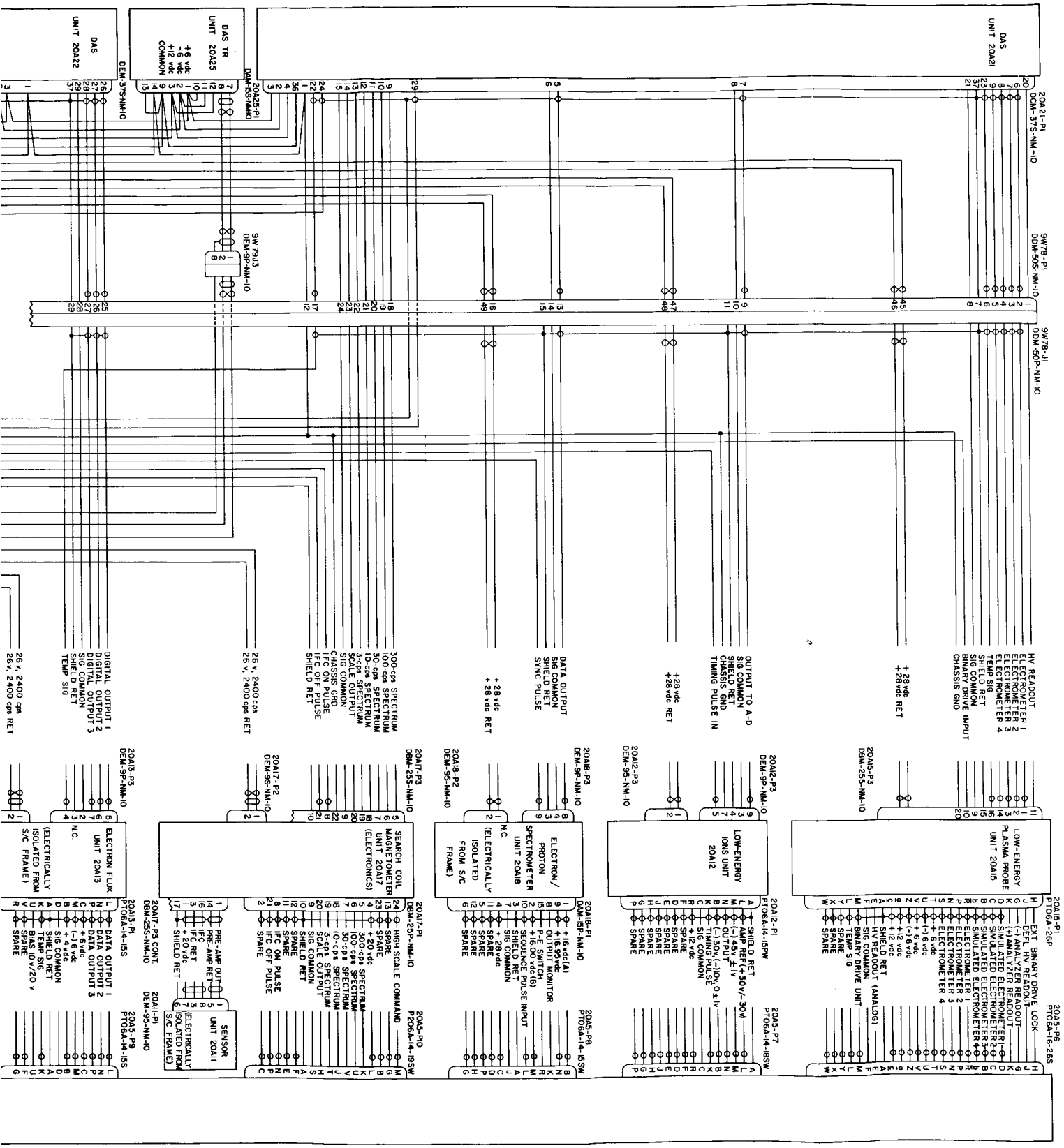


Fig. 5. Systems test cabling master block diagram


DAS UNIT 20A21
DAS UNIT 20A22
DAS TR UNIT 20A23
20A21-P1 DCM-37S-NM-10
20A25-P1 DDM-25S-NMMO
DEM-37S-NM10
9W78-P1 DDM-50S-NM-10
9W78-J1 DDM-50P-NM-10
9W 79-J3 DEM-9P-NM-10
HV READOUT
ELECTROMETER 1
ELECTROMETER 2
ELECTROMETER 3
ELECTROMETER 4
TEMP SIG
SIG COMMON
SHIELD RET
BINARY DRIVE INPUT
CHASSIS GND
+28 vdc
+28 vdc RET
DATA OUTPUT
SIG COMMON
SHIELD RET
SYNC PULSE
+28 vdc
+28 vdc RET
OUTPUT TO A-D
SIG COMMON
SHIELD RET
CHASSIS GND
TIMING PULSE IN
26 v, 2400 cps
26 v, 2400 cps RET
300-cps SPECTRUM
30-cps SPECTRUM
10-cps SPECTRUM
3-cps SPECTRUM
SIG COMMON
CHASSIS GRD
IFC ON PULSE
IFC OFF PULSE
SHIELD RET
DIGITAL OUTPUT 1
DIGITAL OUTPUT 2
DIGITAL OUTPUT 3
SIG COMMON
SHIELD RET
TEMP SIG
+6 vdc
-6 vdc
+12 vdc
COMMON
20A25-P1 DDM-25S-NM-10
20A5-P3 DSM-25S-NM-10
20A15-P1 P106A-26P
20A5-P6 P106A-16-26S
LOW-ENERGY IONS UNIT 20A12
LOW-ENERGY PLASMA PROBE UNIT 20A15
20A12-P3 DEM-9P-NM-10
20A12-P1 PT06A-14-15PW
20A5-P7 PT06A-14-18SW
20A12-P2 DEM-9S-NM-10
20A5-P8 PT06A-14-15SW
20A2-P3 DEM-9S-NM-10
20A18-P3 DEM-9P-NM-10
20A18-P1 DAM-15P-NM-10
ELECTRON/ PROTON SPECTROMETER UNIT 20A18
20A18-P2 DEM-9S-NM-10
20A17-P3 DSM-25S-NM-10
20A17-P1 DBM-25P-NM-10
20A5-P10 P106A-14-18SW
SEARCH COIL MAGNETOMETER UNIT 20A17 (ELECTRONICS)
20A17-P2 DEM-9S-NM-10
20A17-P3 CONT DBM-25S-NM-10
20A11-P1 DEM-9S-NM-10
20A5-P9 PT06A-14-15S
SENSOR UNIT 20A11
20A13-P3 DEM-9P-NM-10
20A13-P1 PT06A-14-15S
ELECTRON FLUX UNIT 20A13
N.C.
(ELECTRICALLY ISOLATED FROM S/C FRAME)
EXT BINARY DRIVE LOCK
HV READOUT
(-) ANALYZER READOUT
(+) ANALYZER READOUT
SIMULATED ELECTROMETER 1-0
SIMULATED ELECTROMETER 2-0
SIMULATED ELECTROMETER 3-0
SIMULATED ELECTROMETER 4-0
ELECTROMETER 1
ELECTROMETER 2
ELECTROMETER 3
ELECTROMETER 4
+6 vdc
(-) 6 vdc
+12 vdc
(-) 12 vdc
SHIELD RET
HV READOUT (ANALOG)
SIG COMMON
BINARY DRIVE UNIT
TEMP SIG
SPARE
SHIELD RET
+16 vdc(A)
+16.95 vdc
OUTPUT MONITOR
+16.00 vdc(B)
SEQUENCE PULSE INPUT
+28 vdc
SPARE
IFC ON PULSE
IFC OFF PULSE
PRE-AMP OUT
PRE-AMP RET
IFC RET
+20 vdc
SHIELD RET
SWITCH SCALE COMMAND
+20 vdc
300-cps SPECTRUM
30-cps SPECTRUM
10-cps SPECTRUM
3-cps SPECTRUM
SIG COMMON
SHIELD RET
(ELECTRICALLY ISOLATED FROM S/C FRAME)

III. THE TELEVISION EXPERIMENT

The primary scientific objective of the *Ranger* Follow-On mission is the acquisition of lunar topographic information of sufficient quality to aid in determining the design of lunar unmanned vehicles and the initial manned lunar exploration program. This objective will be accomplished by the television experiment, which utilizes six 1-in. vidicon cameras arranged as two wide-angle cameras designated Cameras A and B and four narrow-angle, high-resolution cameras designated Cameras 1, 2, 3, and 4. In addition, Camera A is supplied with a color wheel containing three color filters and a single neutral density filter. A different filter is sequentially positioned in the optical path for each exposure.

Cameras A and B are fully scanned, producing a theoretical maximum of 800 TV resolution lines over the tube format (0.44 by 0.44 in.), with a side field coverage of 8.4 deg. The four clustered cameras utilize a reduced raster scanning a 0.11- by 0.11-in. central portion of the tube at the same line density, thus giving a tube format of 200 TV resolution lines as a theoretical maximum. The angular resolution of each camera is then the same. However, the reduced format of the partially scanned system enables a much faster picture cycle; thus more pictures may be taken at lower altitudes than with the fully scanned system.

The type F or fully scanned camera utilizes 1152 active horizontal scan lines over the 0.44- by 0.44-in. faceplate area. The horizontal scan rate is 450 cycles with 0.22 millisec appropriated to horizontal blanking. The time required to cover the active scan lines, plus 46.6 millisec for vertical blanking, makes up the 2.56-sec frame period. At the end of its active scan, the Type F camera enters an erase phase which occupies an equal amount of time. In the *Ranger* television system, two type F cameras are alternately scanned and erased in such a manner that one is being scanned while the other is being erased.

The type P, or partially scanned, camera utilizes 300 active horizontal scan lines over a 0.11- by 0.11-in. faceplate area. The horizontal line rate is 1500 cps, with 111.1 μsec allocated for horizontal blanking. The vertical scan, plus a 6.6-millisec blanking period, takes 0.2 sec. At the end of the vertical scan, an erase procedure is initiated which takes 0.64 sec. In the system, four type P cameras are sequentially scanned; while one is being scanned the remaining three are in various portions of their erase cycles. A 40-millisec pulse is used to separate each sequence of four type P camera exposures.

A controlled programmer and camera sequencer is the central signal generating subassembly which connects the command link interface to the TV payload. It contains the preprogram clocks that initiate the TV system operating sequence signals during terminal maneuver, sync, and time base generating circuits, and the special tone and code signals for the A camera and the camera switchover function. The three video combiners mix the video signal with a sync-toned code and blanking signals to provide the composite video output to the transmitters. The combiners also contain a video pre-emphasis circuit, a corresponding de-emphasis circuit being located in the ground receiver. Transmitter 1 is centered about 959.5 Mc; transmitter 2 is centered about 960.5 Mc, with 1 Mc of RF bandwidth. Each transmitter accommodates about 200 kc of video bandwidth, with engineering telemetry carried on a subcarrier oscillator at 225 kc. Table 1 presents a summary of the camera parameters.

Table 1. Camera characteristics

Characteristics	Cameras A and B	Cameras 1, 2, 3, and 4
Aspect ratio	1 to 1	1 to 1
Active scan area	0.44 x 0.44 in.	0.101 x 0.101 in. (2, 3, 4)
Line rate	450 cps	1500 cps
Horizontal line time	2.22 millisec	666.6 μsec
Horizontal blanking	0.22 millisec	111.1 μsec
Frame rate	0.39 cps	5 cps
Frame time	2.56 sec	0.2 sec
Vertical blanking	46.6 millisec	6.6 millisec
Group vertical blanking		40 millisec
Video bandwidth	200 kc	200 kc
Exposure time	0.005 sec	0.004 sec
F/no.	2	2

At impact minus 55 min, the spacecraft performs a terminal maneuver, after which the cameras are in the proper orientation with the expected velocity vector at impact. At impact minus 15 min, the TV payload warmup mode is initiated. After 5 min of warmup, the complete payload begins to operate at full power, and pictures are then transmitted. At this time, the spacecraft is approximately 1400 km above the lunar surface. At impact minus 1 min, the wide-angle cameras are discon-

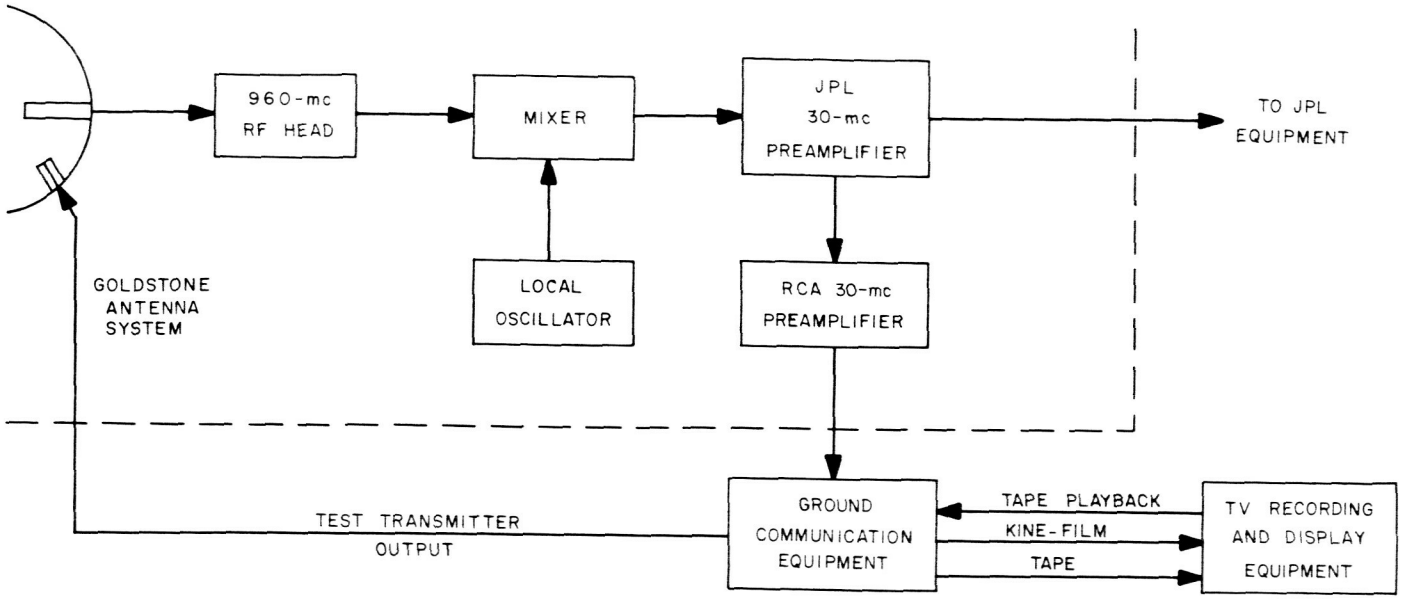


Fig. 7. Goldstone DSIF interconnection block diagram

tinued, and the output of the narrow-angle cameras is sent over both transmitting channels to give data redundancy. The P cameras then operate until impact; owing to their fast readout capability the need for an altimeter is eliminated.

Figure 7 shows the interconnection diagram for the RCA ground support equipment with JPL equipment. The FM signal in the 960.05 ± 1-Mc region is mixed down to the first intermediate frequency in the 30-Mc region. From there it is applied to a 30-Mc RCA preamplifier and a dual-channel limiter amplifier which separates and mixes the two transmitter channels down to 4.47 and 5.53 Mc, respectively. The signals from each channel are further divided so that each goes to a record intermediate frequency amplifier where the signal is converted to a frequency of 0.5 Mc and recorded on magnetic tape, a detector amplifier from which the signal is applied to a 225-kc discriminator unit which accepts only the telemetry data, and a low-pass filter from which the TV data are recorded on 35-mm film by a kinescope camera. Thus, the TV data from each channel are recorded on magnetic tape and 35-mm film. The 35-mm film format is shown in Fig. 8, with P cameras numbered in sequence and A and B cameras labeled appropriately.

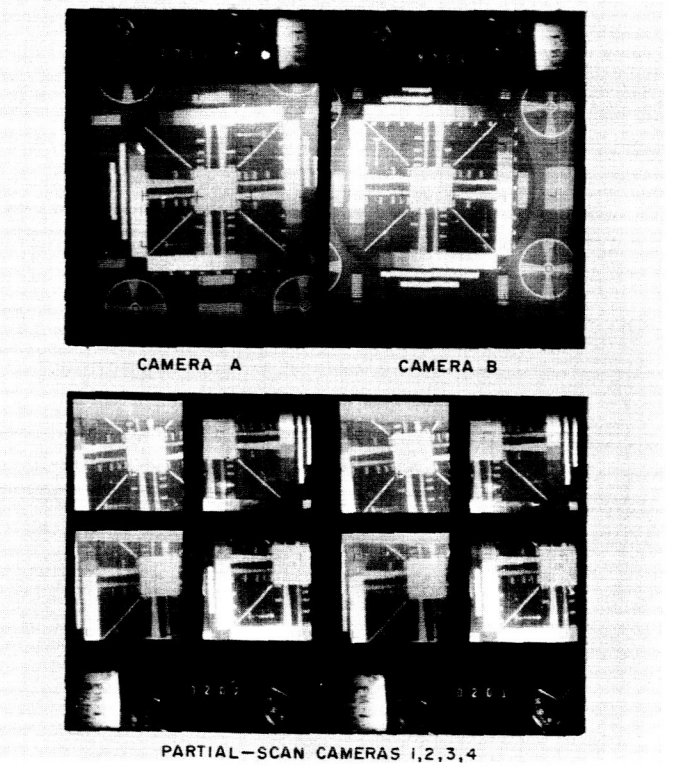


Fig. 8. TV camera format

IV. SCIENCE TRANSFORMER RECTIFIER

The science TR unit (Fig. 9) supplies 52-v, 2400-cps, and 28-vdc power used by science experiments and the DAS. The 2400 cps from the science inverter is coupled through transformer T3 to four fused outputs for the experiments. The secondary of transformer T3 is tapped to the primary of transformer T2, which couples a portion of the signal to the current limiter, consisting of transistor Q1 and its associated circuitry. The current limiter was designed to regulate the initial surge current to a value low enough so that the safety fuses would not be blown. The secondary of transformer T3 is also coupled through transformer T1 to three full-wave rectifiers which provide three separate 28-vdc outputs. The 28-vdc outputs are also fused for protection.

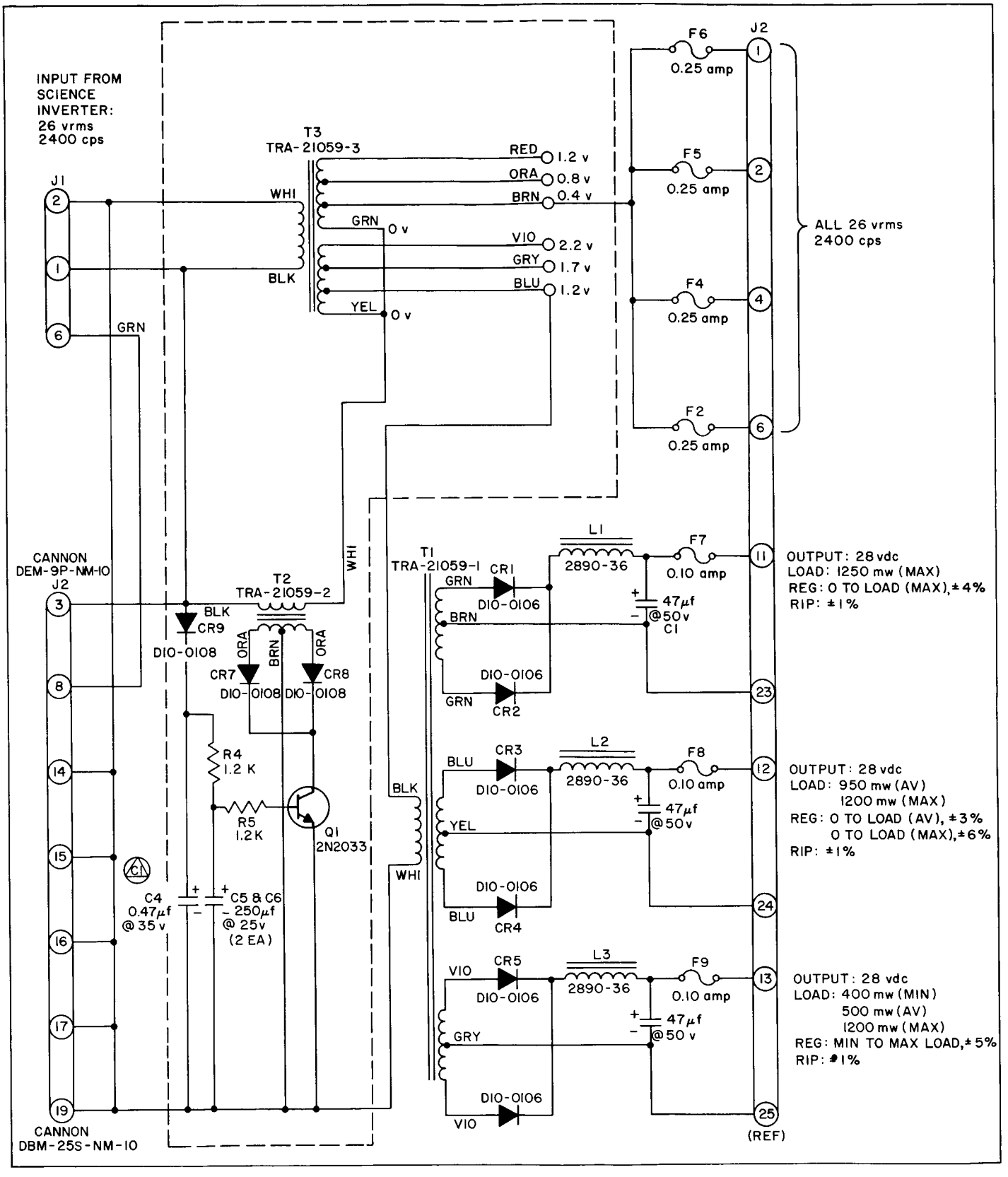


Fig. 9. Science transformer rectifier schematic diagram

V. COSMIC DUST EXPERIMENT

The cosmic dust detector (Fig. 10 and 11) will measure the density and momentum of dust particles with masses between about 10^{-13} to 10^{-6} gm and thus will increase our knowledge concerning the dust particle distribution in the Earth-Moon system. It also may provide information concerning the Moon as a possible source of micron-size

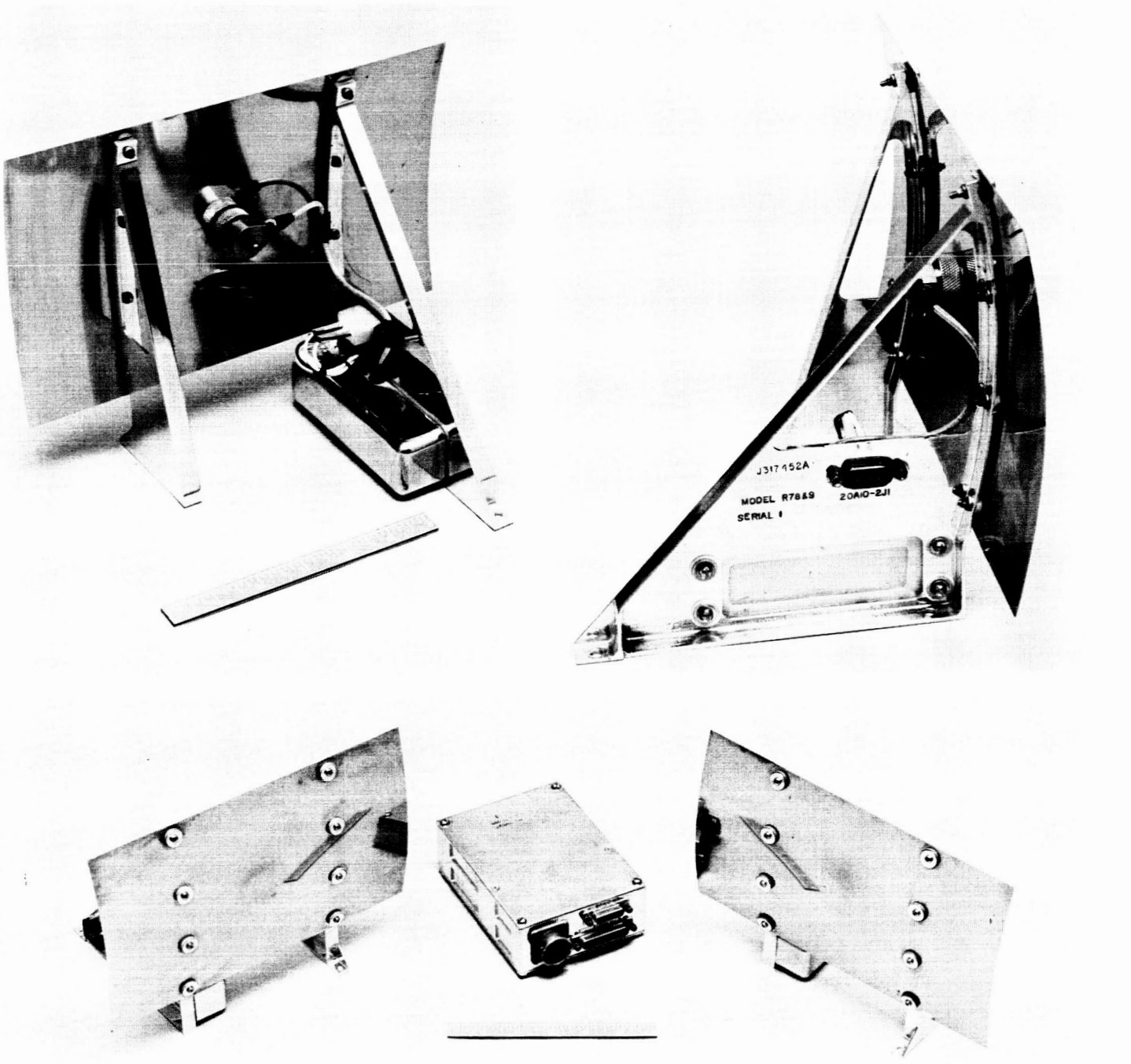


Fig. 10. Cosmic dust experiment

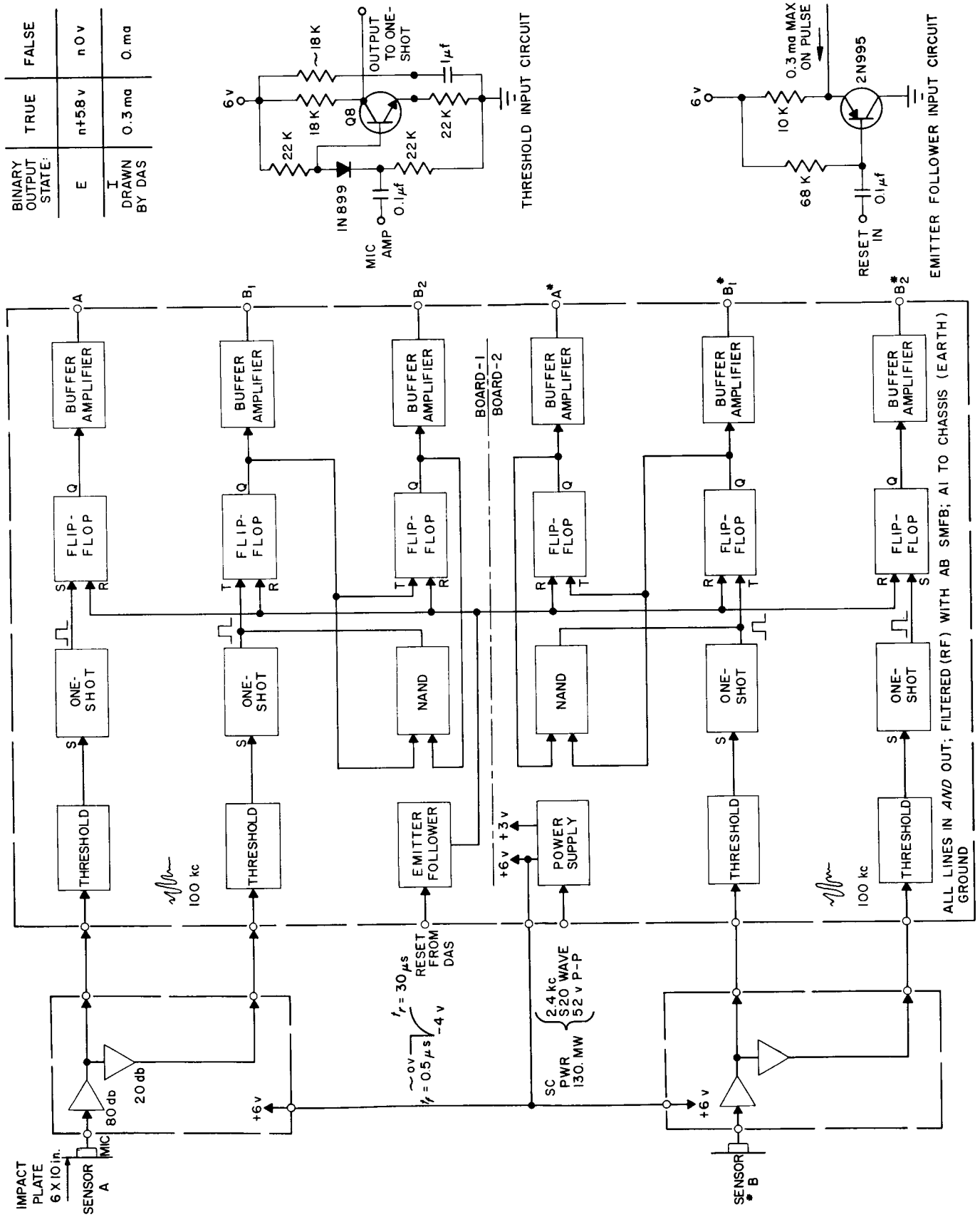


Fig. 11. Cosmic dust detector block diagram

dust particles, information which is important to the manned spaceflight effort. The experiment contains two independent acoustical transducers which are piezoelectric 100-kc crystals bonded to the geometric center of metallic plates. The sensors detect micron-size dust particles impacting on the plates. The 6- by 10-in. stainless-steel plates exposed to impacts are mounted opposite each other on the spacecraft and perpendicular to the ecliptic plane.

A dust particle impacting onto the exposed plate produces a mechanical impulse which is coupled to the acoustical transducer. The resultant electrical pulse from the crystal is amplified by a tuned amplifier having a center frequency of 100 kc and a 10-kc bandpass. The overall gain of the amplifier is 100 db, with an output tap at 80 db. Calibration of the experiment in the laboratory consists of dropping ruby spheres onto the impact plate, with a sensitivity expressed in units of momentum.

A. The Electronics

The output of the crystal transducer is ac coupled to the preamplifier and driver circuitry shown in Fig. 12. Transistors Q1 through Q4 constitute a 100-kc tuned amplifier with 80-db voltage gain. This output is directly coupled to an emitter follower Q6, which drives the threshold circuits. Transistor Q5 is used to give an addi-

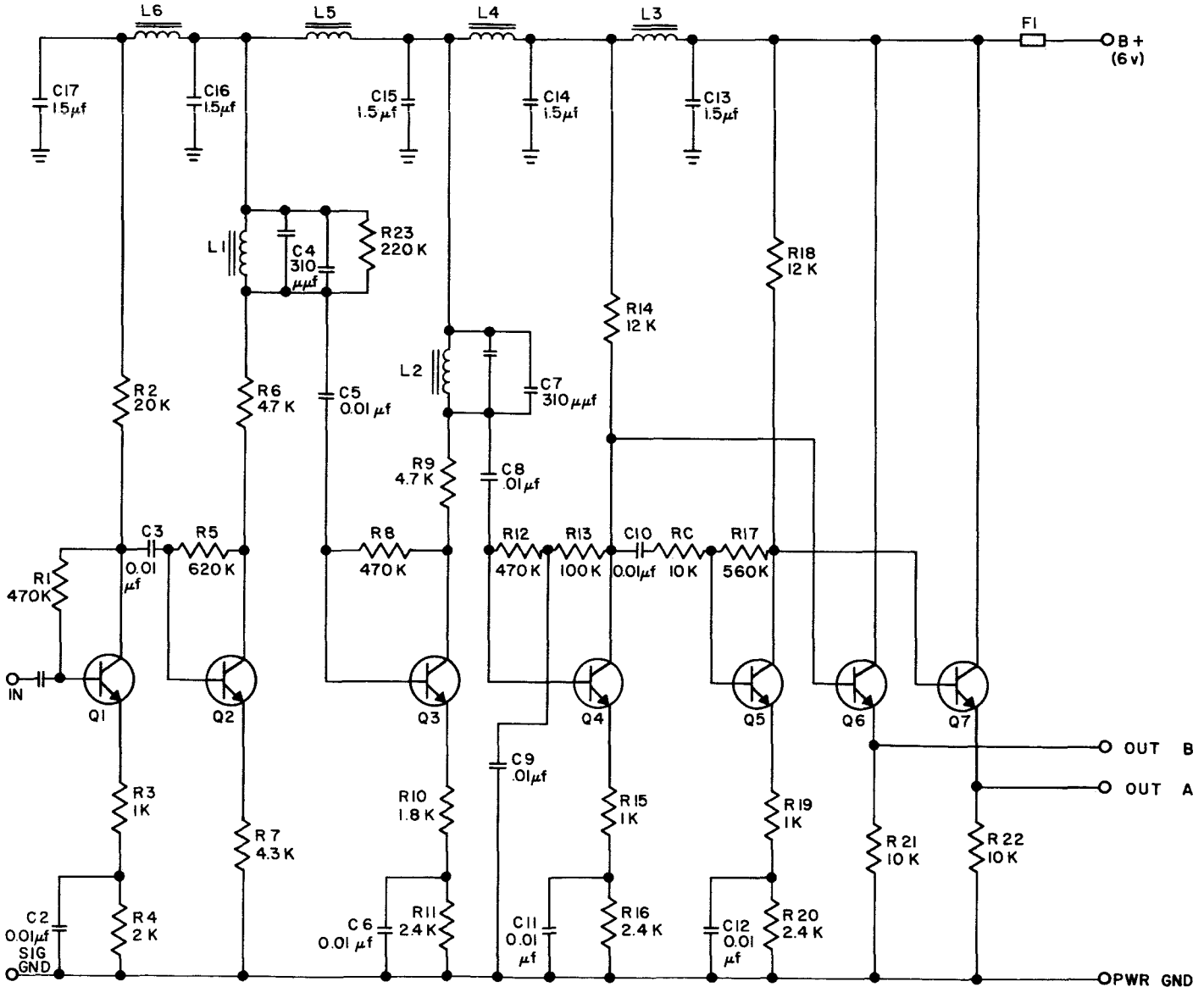


Fig. 12. Cosmic dust experiment preamplifier schematic diagram

tional 20-db gain to the signal from Q4. This signal is also coupled to an emitter follower Q7, which drives a threshold circuit. The threshold circuit is shown to the right of the block diagram in Fig. 11. In the quiescent condition, Q8 is turned off by the voltage divider, consisting of the 18 and the 22K resistors. When the input signal from the preamplifier exceeds 0.7 v, diode 1N899 is reverse biased, and Q8 becomes forward-biased and produces a negative-going output signal. The threshold output is coupled through capacitor C3 to the one-shot shown in Fig. 13. The signal reverse biases CR1, which turns Q2 on and Q1 off. The 0- to 6-v output pulse is then taken from the collector of Q1 and fed to the toggle input of the flip-flop shown in Fig. 14. The one-shot pulse output turns flip-flop transistor Q1 off, and the resulting 6-v level taken from the collector of Q1 reverse-biases diode CR1 of the buffer amplifier shown in Fig. 15. Buffer transistor Q1 is turned on, thus turning off output transistor Q2, which presents the DAS a 6-vdc level through isolation resistor R4.

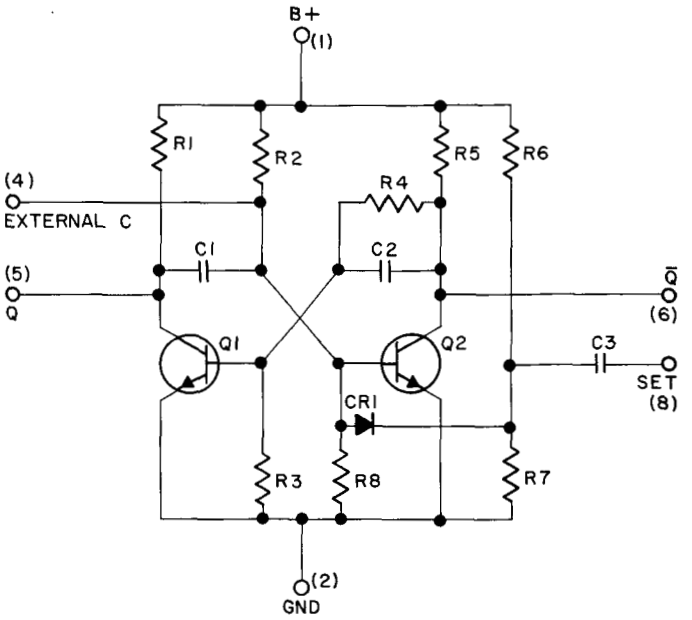


Fig. 13. Cosmic dust experiment monostable multivibrator schematic diagram

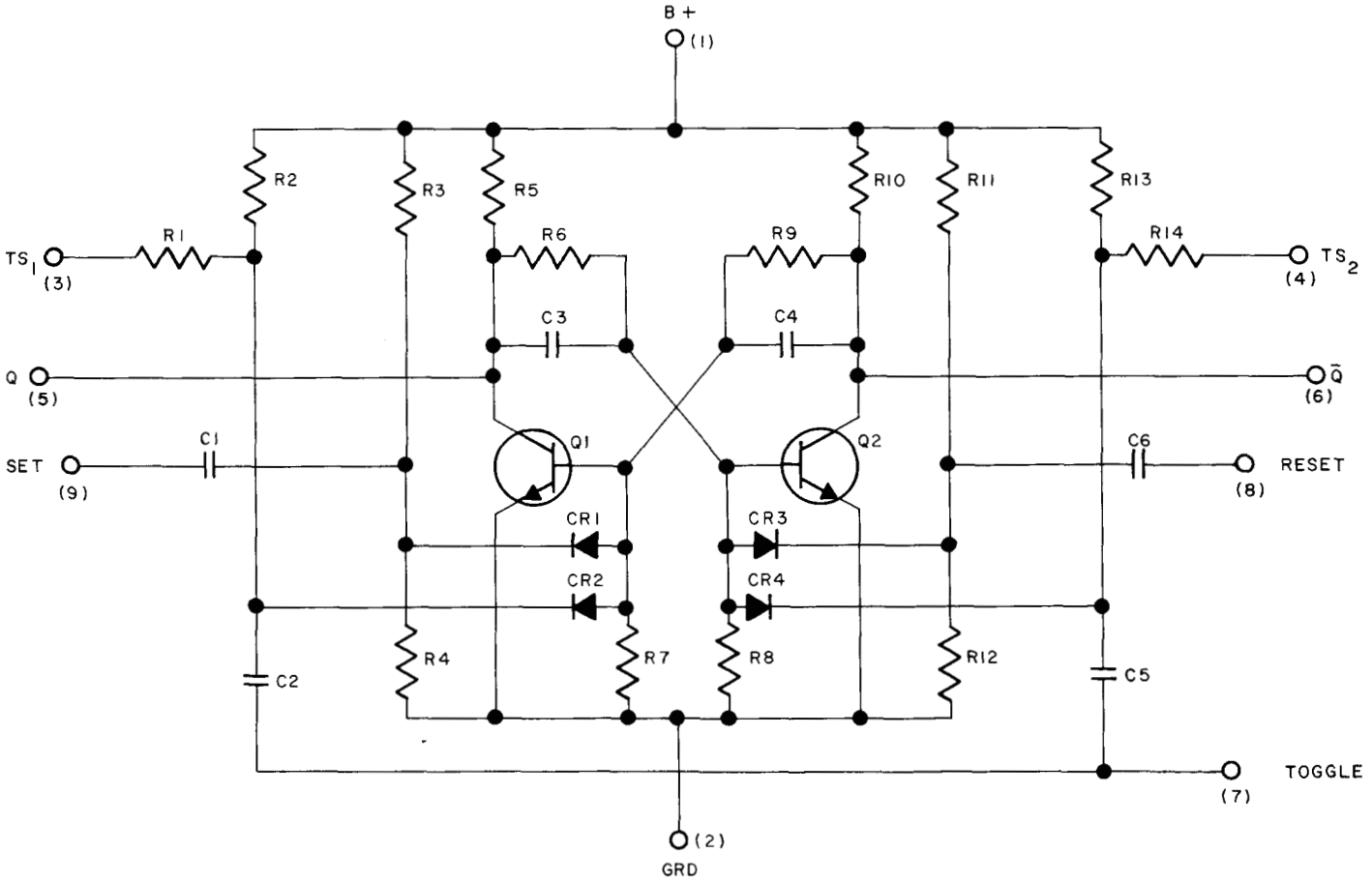


Fig. 14. Cosmic dust experiment bistable multivibrator schematic diagram

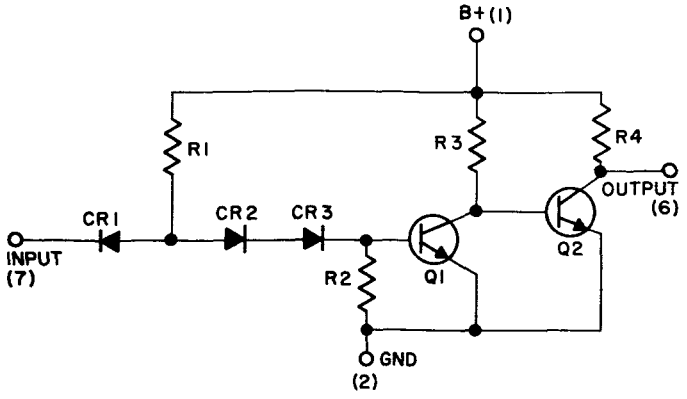


Fig. 15. Cosmic dust experiment buffer amplifier schematic diagram

Referring to the block diagram in Fig. 11, the flip-flops associated with outputs B1, B2 are used as a binary counter and, with one low-level impact, B1 is true and B2 is false. When two low-level impacts occur, B1 flip-flop is retriggered to 0, which in turn sets flip-flop B2 to its true state. As a third impact is recognized, B1 is then set to its true state while B2 remains in its true state. (Flip-flops are triggered by a negative-going signal.) When both B1 and B2 are true, the outputs from these flip-flops are also coupled to the *nand* gate shown in Fig. 16. This reverse-biases CR1 and CR2, which turns both Q1 and Q2 on. The *nand* gate output is coupled to the output of the one-shot, and when Q2 is turned on, the one-shot output is coupled to ground. This circuitry is utilized to ensure that the binary counter does not receive any more than 3 pulses during any given sampling time, since any more impacts would render invalid all information previously received. All the flip-flops are reset by a trigger pulse from the DAS, which occurs every 40.32 sec. This reset pulse is coupled through the emitter-follower input circuitry shown in Fig. 11.

B. The Power Supply

The 3- and 6-v bias required by the cosmic dust detector is derived from the circuitry shown in Fig. 17. A 52-v peak-to-peak squarewave from the science TR unit is transformer-coupled, fullwave-rectified by diodes CR1 and CR2, and then filtered by a conventional RC network. Zener diode CR5 is used for voltage regulation. The +3 v is derived in the same manner, except that there is no zener diode regulation, and the capacitor filtering is located external to the power supply.

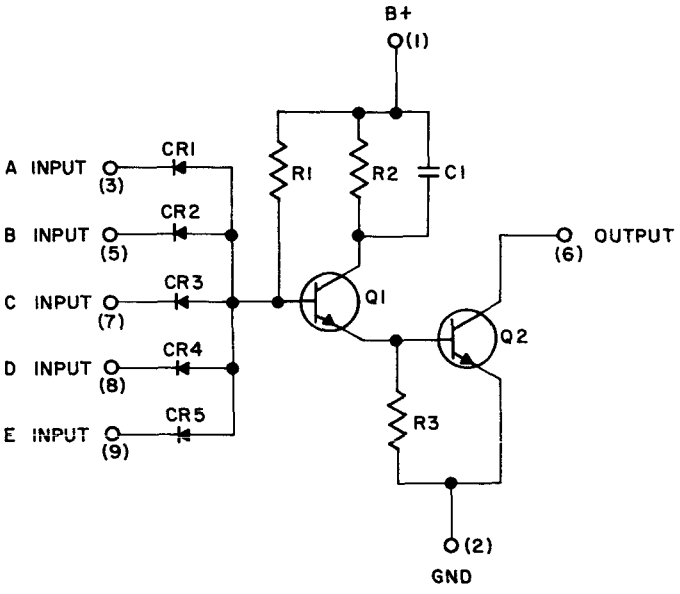


Fig. 16. Cosmic dust experiment *nand* gate schematic diagram

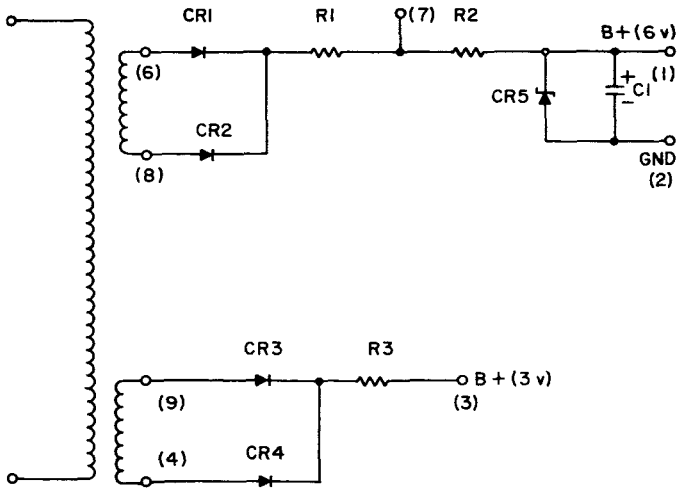


Fig. 17. Cosmic dust experiment power supply schematic diagram

VI. LOW-ENERGY SOLAR PLASMA EXPERIMENT

The scientific objective of the low-energy solar plasma experiment is to detect low-energy protons in a solar plasma while outside the geomagnetic field. The instrument will detect the magnitude and direction of the proton flux in the energy range of 500 to 20 kev. It has been calculated that the presence of the Earth's dipole field significantly distorts any interplanetary field out to a distance of some 40 Earth radii in the absence of plasma. Knowledge of the plasma flux gradient between the Earth and Moon is essential if one is to understand the complex relation between the plasma and the field, and it will be extremely significant to determine the plasma flux outside of the Earth's magnetic influence.

The instrument is a curved-plate electrostatic analyzer. Charged particles entering the analyzer are deflected by an electric field which is approximately transverse to the particle velocity. Those particles with positive charge within a certain range of energy per unit charge and angle incidence are deflected onto a collector plate. Particles which enter with a negative charge, wrong energy per unit charge, or wrong angle of incidence strike the analyzer walls and are not recorded. The energy distributions are determined by varying the magnitude of the deflection voltages. With a split area of about 1 cm^2, the minimum detectable current of 10^{-14} amp corresponds to a maximum sensitivity of 10^5 to 10^6 particles per cm^2 per sec, depending upon geometrical factors which are calibrated with laboratory ion beams.

The entire instrument consists of four individual electrostatic plate collector assemblies pointing in four directions spaced 10 deg apart in a common plane. The assemblies have individual electronics and can operate independently except for common power supplies. In addition to the electrostatic plates for separating the particles according to energy, there is a pair of high-voltage plates which allow the instrument to detect particles that do not come straight in. This deflection plate is programmed to look alternately straight ahead and 10 deg off axis.

Each of the four charged collectors serves as the input to separate electrometer amplifiers which provide four analog voltage outputs to the DAS. A fifth analog voltage output indicates the sequencing of the analyzer plate and deflection plate voltages. A sixth analog voltage output indicates the temperature of the unit. Figure 18 is a photograph of the low-energy solar plasma experiment.

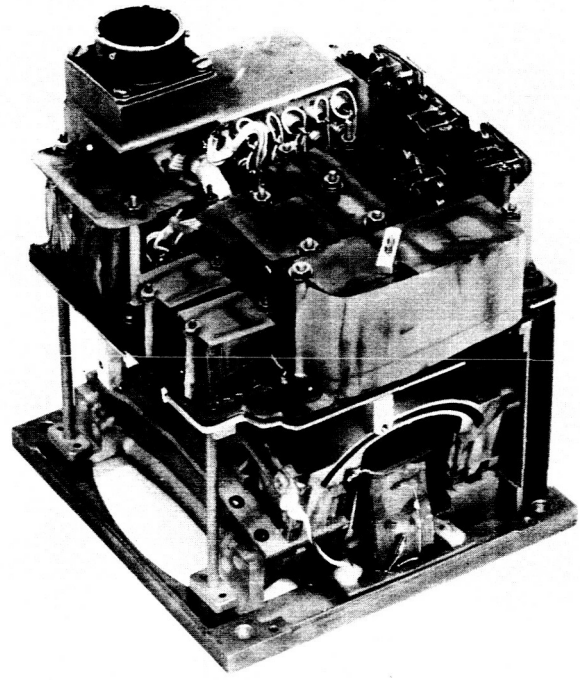


Fig. 18. Low-energy plasma probe experiment

A. The Electronics

The four electrometer amplifiers are shown to the right of the schematic in Fig. 19. The input of each amplifier is directly coupled to the grid of the subminiature electrometer tube. The output of the electrometer is then fed through two stages of emitter followers and two inverting amplifiers. The signal from the inverting amplifier accomplishes two things: first, it charges the RC network of the output amplifier, which in turn produces an analog signal to the data automation system via the output emitter follower; second, it generates feedback to the electrometer tube. The feedback circuit is designed to provide a linear response to 10^{-14} amp and then become logarithmic to cover a dynamic range of 10^5. The operating range of the amplifier is 10^{-14} to 10^{-9} amp. It is calibrated by inserting known currents into the amplifier. An ion beam calibration is made in the laboratory to get the constant of proportionality between particles per cm^2

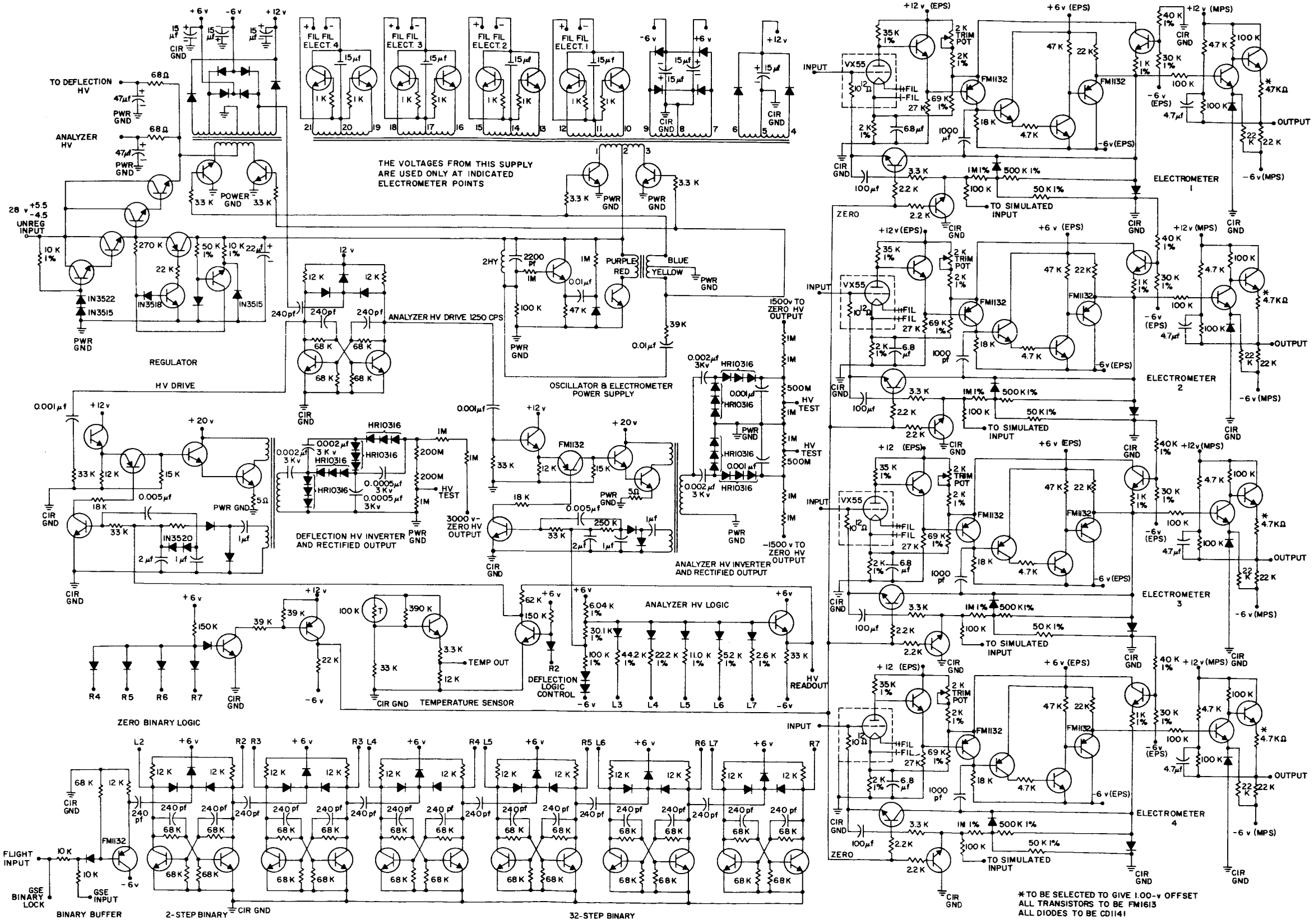


Fig. 19. Low-energy plasma probe schematic diagram

per sec and collector current. The functioning of the amplifiers is checked by applying voltages to the feedback circuit during instrument checkouts. Owing to the feedback nature of the circuit, this test will determine proper operation of all the electronic circuitry.

Deflection plate voltages are controlled by binary pulse commands from the data automation system. The binary commands are buffered by an emitter follower, which in turn drives a two-step binary and a 32-step binary. The first binary alternately turns the 1250-cps drive to the primary of the deflection high-voltage inverter and rectifier on and off. The remaining five flip-flops regulate the voltage amplitude of 1250-cps drive to the primary of the analyzer high-voltage inverter and rectifier. This is accomplished by controlling the base current of the common emitter amplifier shown in the high-voltage analyzer section.

The analyzer high-voltage logic also provides a 0- to 6-v analog signal to the DAS which corresponds to the high-voltage appearing on the analyzer plates. During the last four steps of each data cycle, the zero binary logic *and* gate goes true, and the associated amplifiers provide a 0 calibrate signal to the electrometers to check calibration. A simple thermistor temperature sensor is also employed to record the temperatures within the electronics package. Figure 20 is a block diagram of the experiment, showing the signal flow and the sequence of events.

B. The Power Supply

The unregulated 28 vdc from the science TR unit is first regulated and then used to drive a free-running oscillator. The oscillator output provides base drive to the switching transistors on the primary side of the multitap transformer. Four of the secondaries of the electrometer transformer are current-limited and filtered to provide individual filament voltages to each of the electrometers, while the remaining two windings provide a rectified and filtered dc bias for all of the electrometer amplifiers.

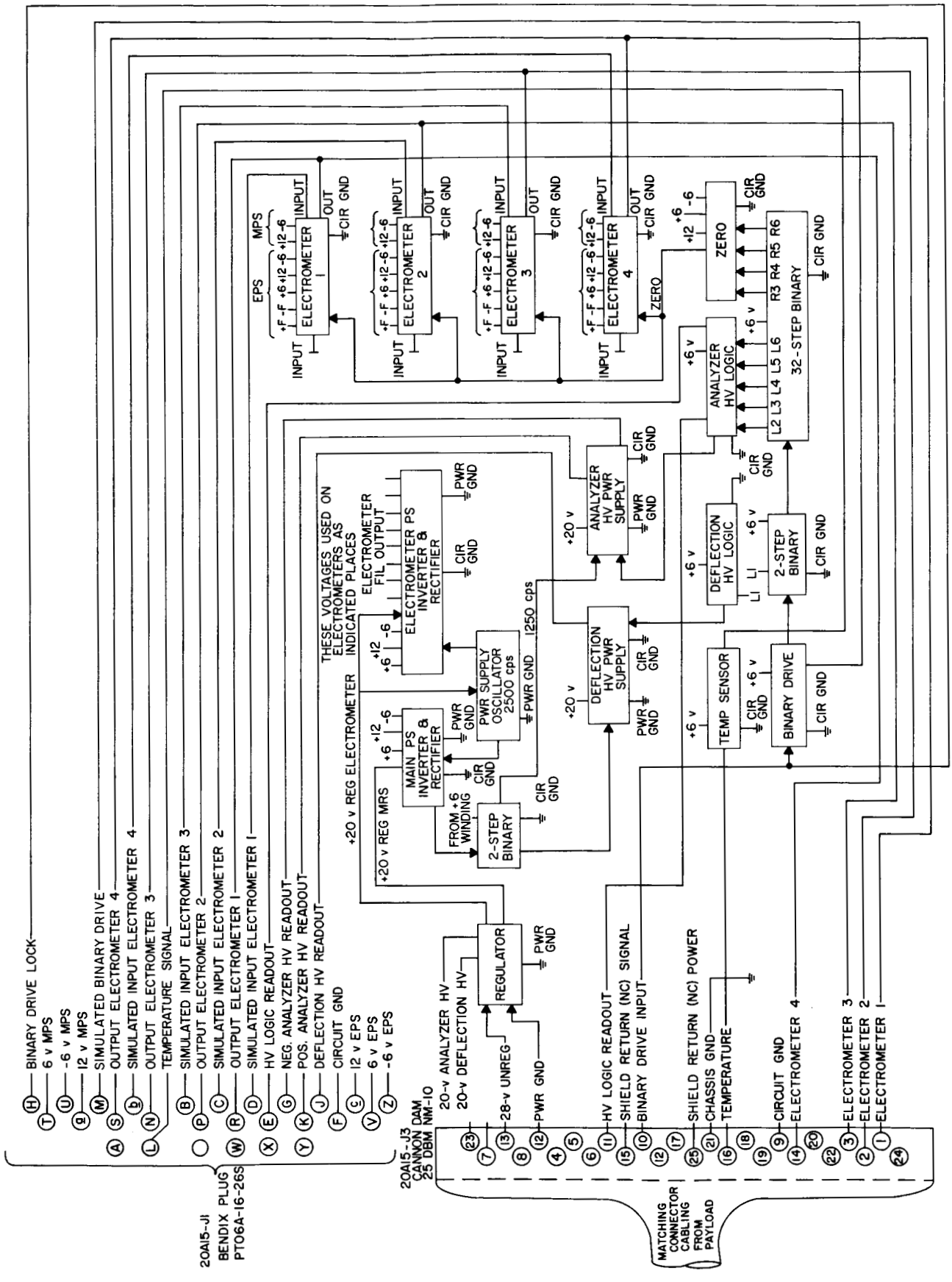


Fig. 20. Low-energy plasma probe block diagram

VII. ELECTRON FLUX DETECTOR EXPERIMENT

The purpose of the electron flux detector is to measure the absolute electron flux in the energy range from 250,000 to 3,000,000 electron volts. To accomplish this, three silicon solid-state detectors of the lithium drifted or surface barrier variety are used. The three detectors are sensitive to electrons and protons in specific energy ranges. As an electron or proton is encountered, a pulse whose amplitude is proportional to the particle's energy is generated by the detector. This pulse is then fed to a preamplifier-amplifier combination followed by a single-channel pulse height analyzer. Figure 21 is a photograph of the electron flux detector experiment.

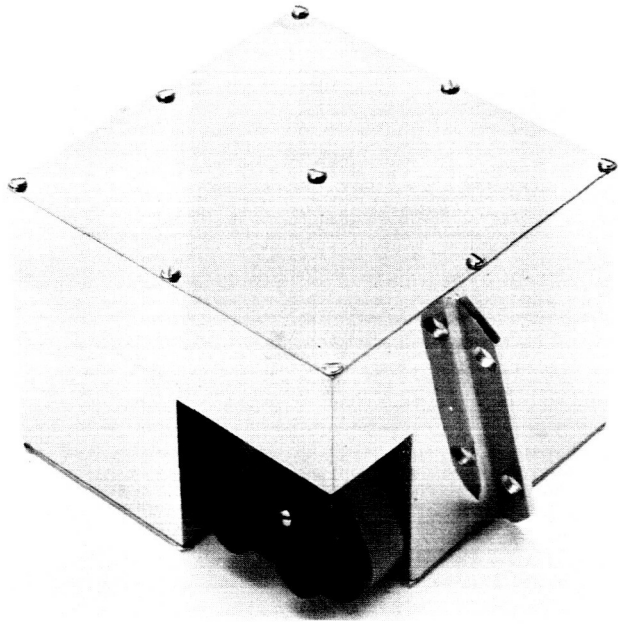


Fig. 21. Electron flux detector experiment

A. Description of the Detectors

All detectors are shielded with copper in all directions except for the 60-deg full-angle entrance aperture. Detectors A (active) and BH (high-energy background) have a sensitive depth of 1 mm, while the BL (low-energy background) detector has a sensitive depth of only 5 microns. Among the several sources of background are low-energy protons which would fall within the energy range to be measured by this experiment. To reduce this contribution, 11.2 mg per cm^2 of aluminum is placed in the entrance aperture of detector A. This absorber will stop a 2-mev proton, and only protons between 2.07 and 2.29 mev will be counted. The effect of this aluminum absorber on electrons is just to increase the lower energy limit from 250 to about 280 kev. Detector BL is shielded in exactly the same way as the active detector A, including the aluminum absorber; but, because its depletion layer is very thin, it is insensitive to electrons. Such a shielded detector, having a depletion layer of 5 microns, will stop approximately 27-kev electrons and is sensitive to protons only in the range of interest, 2.07 to 2.29 mev.

Figure 22 shows the electron and proton energies which will be counted by the active detector. The counting rate in detector BL can be subtracted directly from the counting rate in detector A. Detector BH serves two purposes: first, it sets the upper electron energy limit for the system to 3 mev through the use of a copper absorber; second, it makes possible the elimination of the background due to minimum ionization protons incident normally and other particles which penetrate the shielding. With the energy ranges of each detector as specified, and after subtraction of the counting rates of the BH and BL detectors from that of the A detector, only those events due to electrons between 0.25 and 3 mev remain.

B. The Electronics

Figure 23 is a block diagram of the electron flux detector; Fig. 24 presents several schematic diagrams of the detector. A bias of 200 v for the A and BH detectors and 10 to 20 v to the BL detector is applied from the power supply to achieve depletion through to the rear surfaces of the detectors. A detected particle initiates a pulse to the input of the charged sensitive preamplifier consisting of Q1 and Q2. This output is coupled to the emitter follower Q3 and is then fed through 2 stages of voltage amplifiers consisting of transistors Q4 through Q7. The lower limit of the pulse height analyzer is set up with resistors R1 and R2, thus biasing the base of Q1 to approximately 0.94 v. The upper limit of the analyzer is controlled by the voltage divider consisting of R6 and R7. This reverse biases the base of Q3 in the flip-flop section. The upper limit is adjusted for approximately 3 v. When a pulse between these limits is received from the third amplifier stage, Q1 conducts. This pulse is then amplified by Q5, coupled to the emitter follower Q6, which in turn triggers the one-shot section consisting of

Q7 and Q8. The output of Q8 is then amplified by Q9, and the emitter follower Q10 provides the low output impedance necessary to drive succeeding cables and DAS input circuits. The pulse from the third-stage amplifier is also differentiated by a C2 and R7. When the differentiated pulse height exceeds the upper limit, transistor Q3 of the flip-flop section is turned on. This increases the reverse bias on the collector of Q5 to the point at which Q5 will not be triggered by the output of Q1. As the pulse falls back through the lower limit, flip-flop Q3 and Q4 is reset and the circuit is ready to receive another pulse.

C. *The Power Supply*

The primary power used by this experiment is a 2400-cps squarewave received from the science TR unit. The squarewave is transformer-coupled to appropriate RC rectifier sections which produce the dc voltages used for the circuitry and the detectors in this experiment. Figure 25 is a schematic diagram of this power supply.

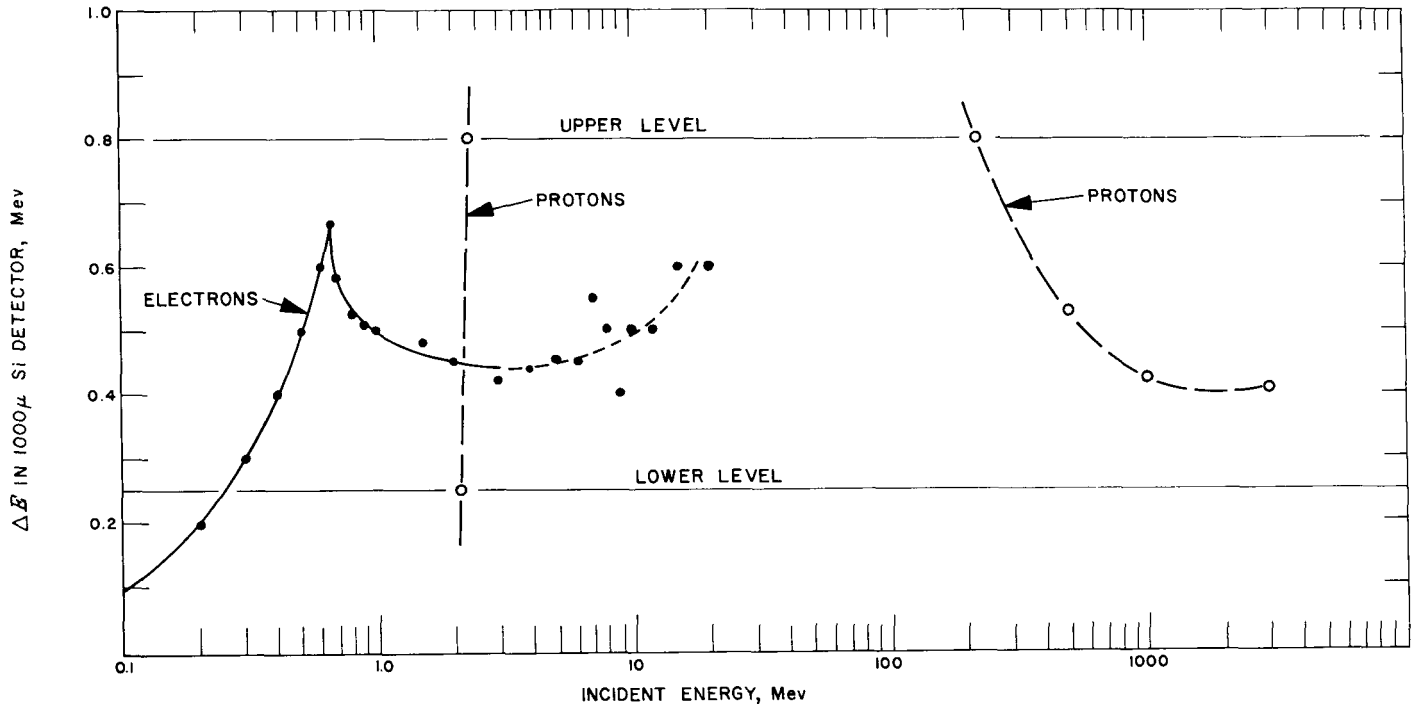


Fig. 22. Electron flux detector experiment energy sensitivity

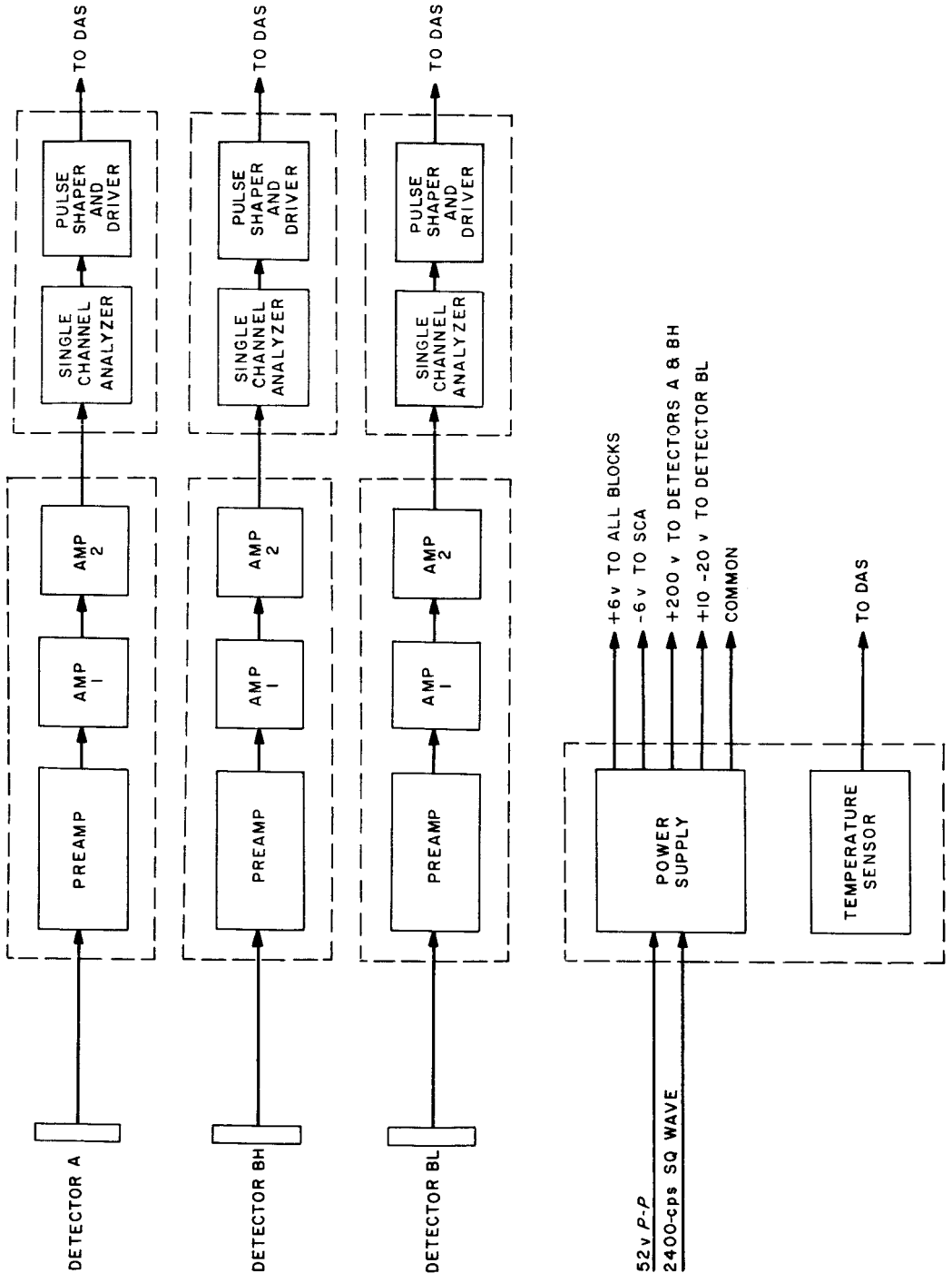


Fig. 23. Electron flux detector experiment block diagram

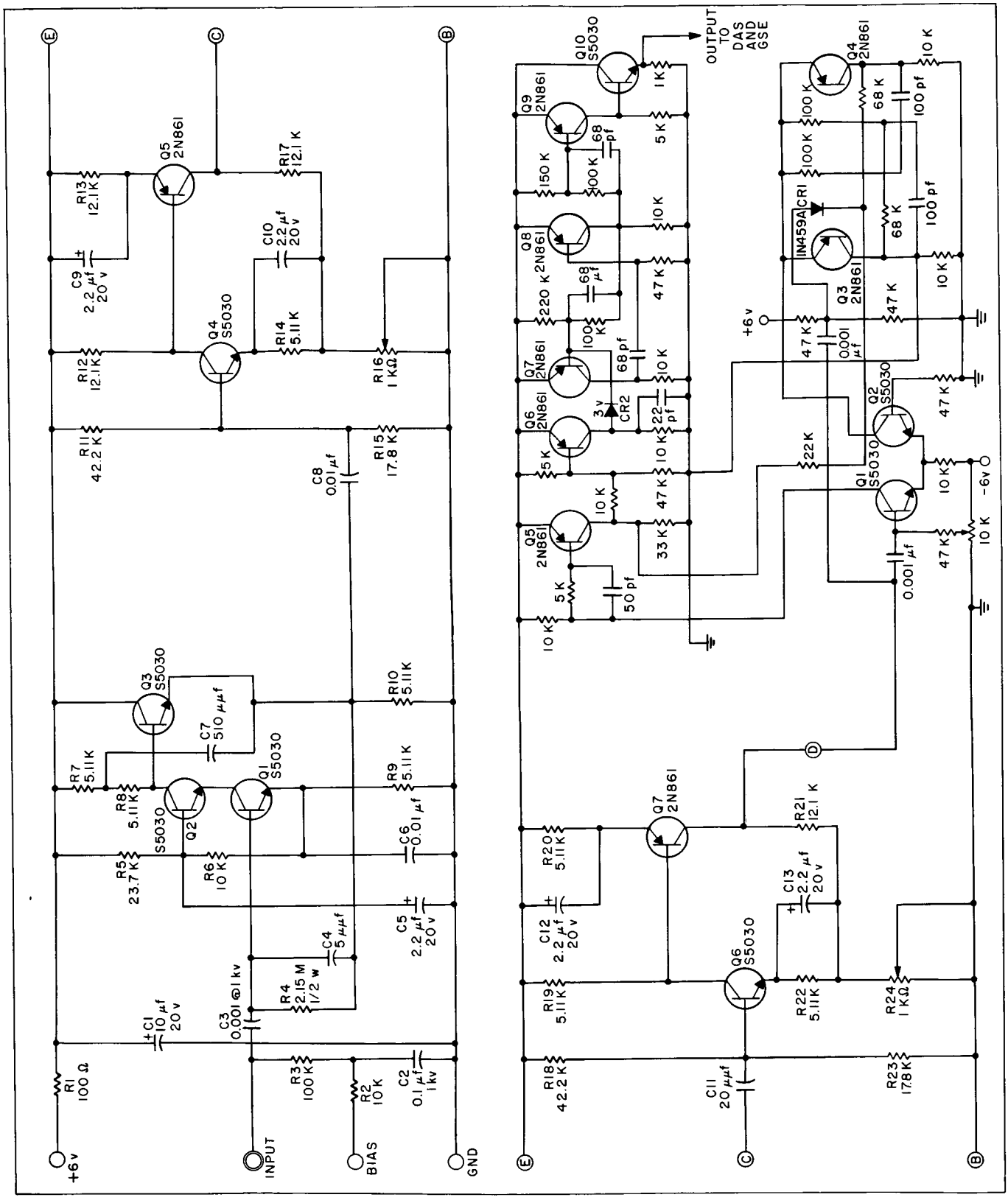


Fig. 24. Electron flux detector experiment schematic diagram

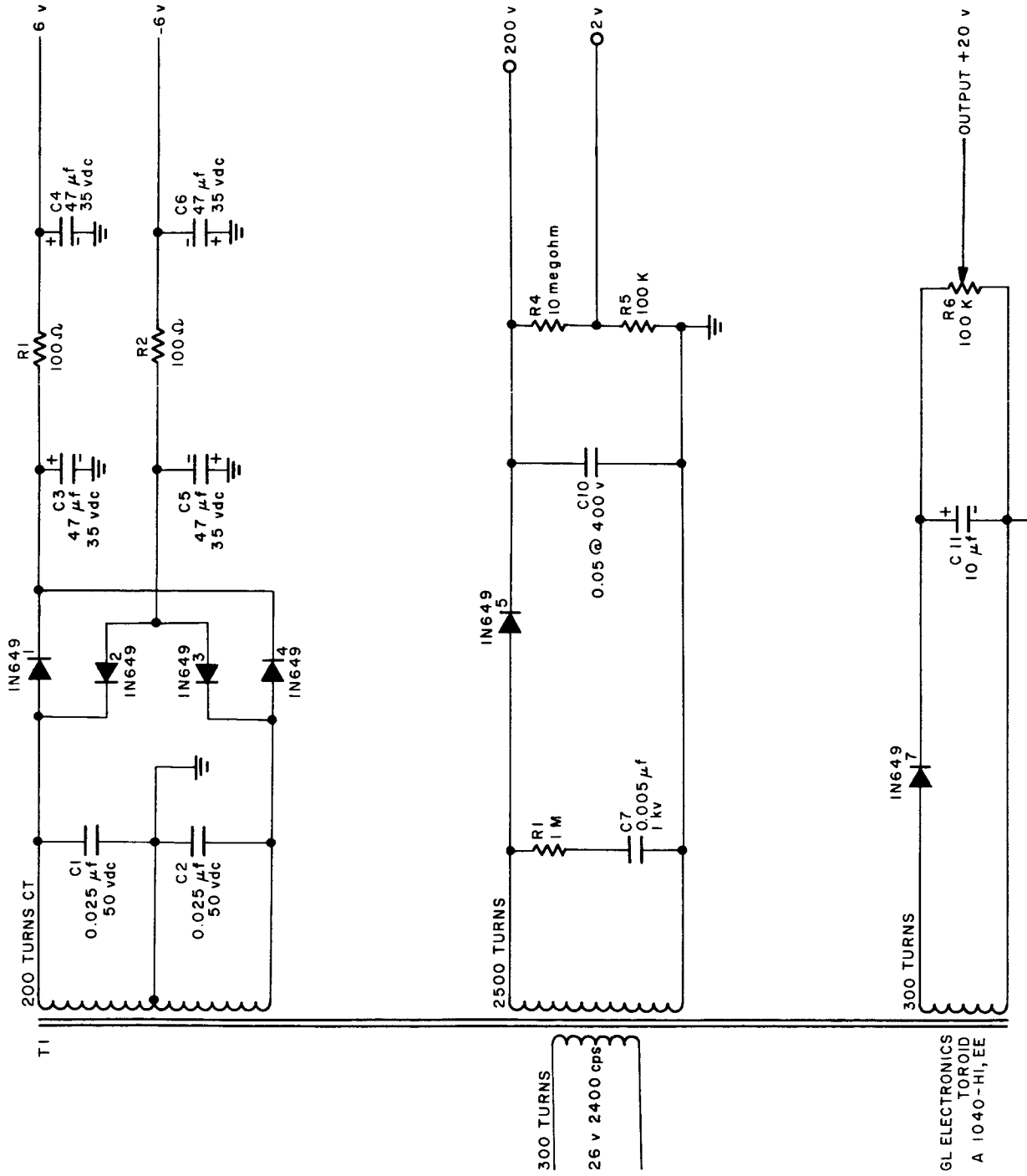


Fig. 25. Electron flux detector experiment power supply schematic diagram

VIII. ELECTRON-PROTON SPECTROMETER EXPERIMENT

The primary scientific objectives of this experiment are to search for neutron decay electrons which may exist in space during solar quiet periods and also to determine to what extent the solar wind plasma contains extremely hot protons. The instrument will unambiguously separate electrons from protons and measure the fluxes and energies of each in the range of 80 to 800 kev for electrons and 800 kev to 5 mev for protons. The detector for this experiment is a single photomultiplier tube with a plastic scintillator and a cesium iodide crystal mounted on its face. The separation of electron and proton pulses is accomplished by means of pulse-shaped discriminator circuits. The input pulses are further analyzed by means of an 8-channel differential pulse height analyzer, and counts in each channel are stored in analog form as charges on a capacitor. Two temperature sensors are provided to indicate temperatures of the photomultiplier tube and the amplifier assembly. The ten channels of analog data are then read out in response to sequence pulses from the DAS, which converts the analog voltages to digital signals for transmission by the telemetry system. Photographs and a block diagram of the electron-proton spectrometer experiment are presented in Fig. 26 and 27, respectively.

A. The Detector

The detector consists of a photomultiplier tube, on the face of which is cemented a 1-mm-thick cesium iodide crystal. Over this is cemented a thin plastic scintillator. The assembly is covered with two layers of aluminized mylar foil to exclude light. Protons striking the detector produce a pulse at the photomultiplier output having a fast rise time due to the short decay of the fluorescence of the plastic scintillator. Electron pulses have virtually no fast rising portion because of the very small amount of energy which they lose in the plastic scintillator. The anode and last dynode outputs from the RCA 7151 photomultiplier tube are coupled to a fast pulse detector circuit and a delay multivibrator in the electronics package as shown in the block diagram in Fig. 27.

B. The Electronics

The signal taken from the anode of the photomultiplier tube is heavily differentiated and amplified by an amplifier having a bandwidth of several hundred megacycles. This fast pulse detector amplifier includes transistors Q1 through Q8 of the schematic in Fig. 28. This circuit controls a decision gate (transistors Q12 through Q15). The trigger of this gate is adjusted so that only protons operate it. The signal from the last dynode, transistor Q2, is the second input to the decision gate and is indicated on Fig. 28 as S1, S2 drive. When it is desired to count electrons, the gate is operated normally open and is closed by outputs from the fast amplifier to exclude protons. This is accomplished by the action of

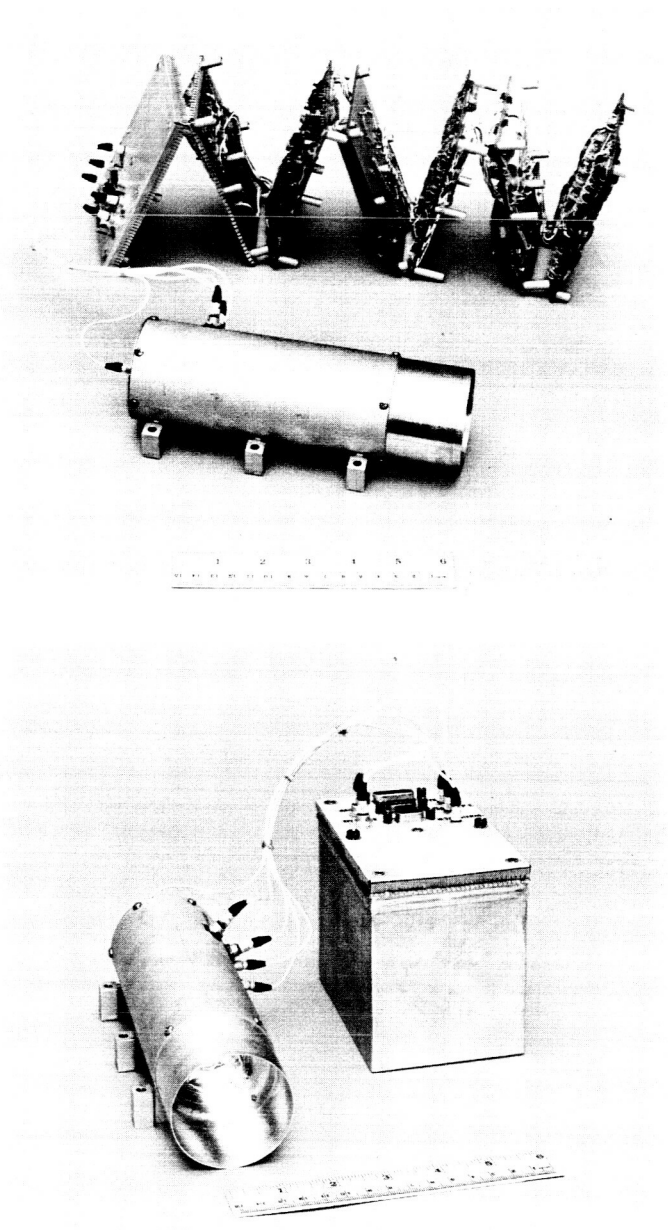


Fig. 26. Electron-proton spectrometer experiment

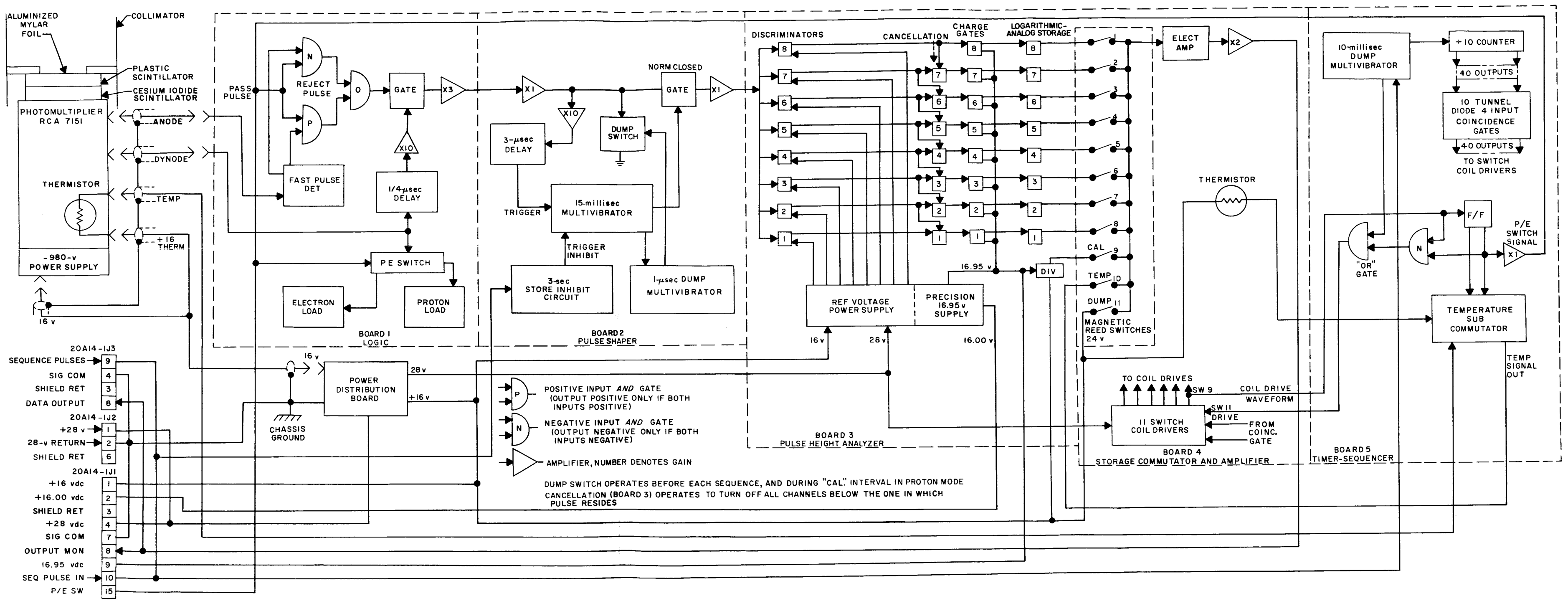
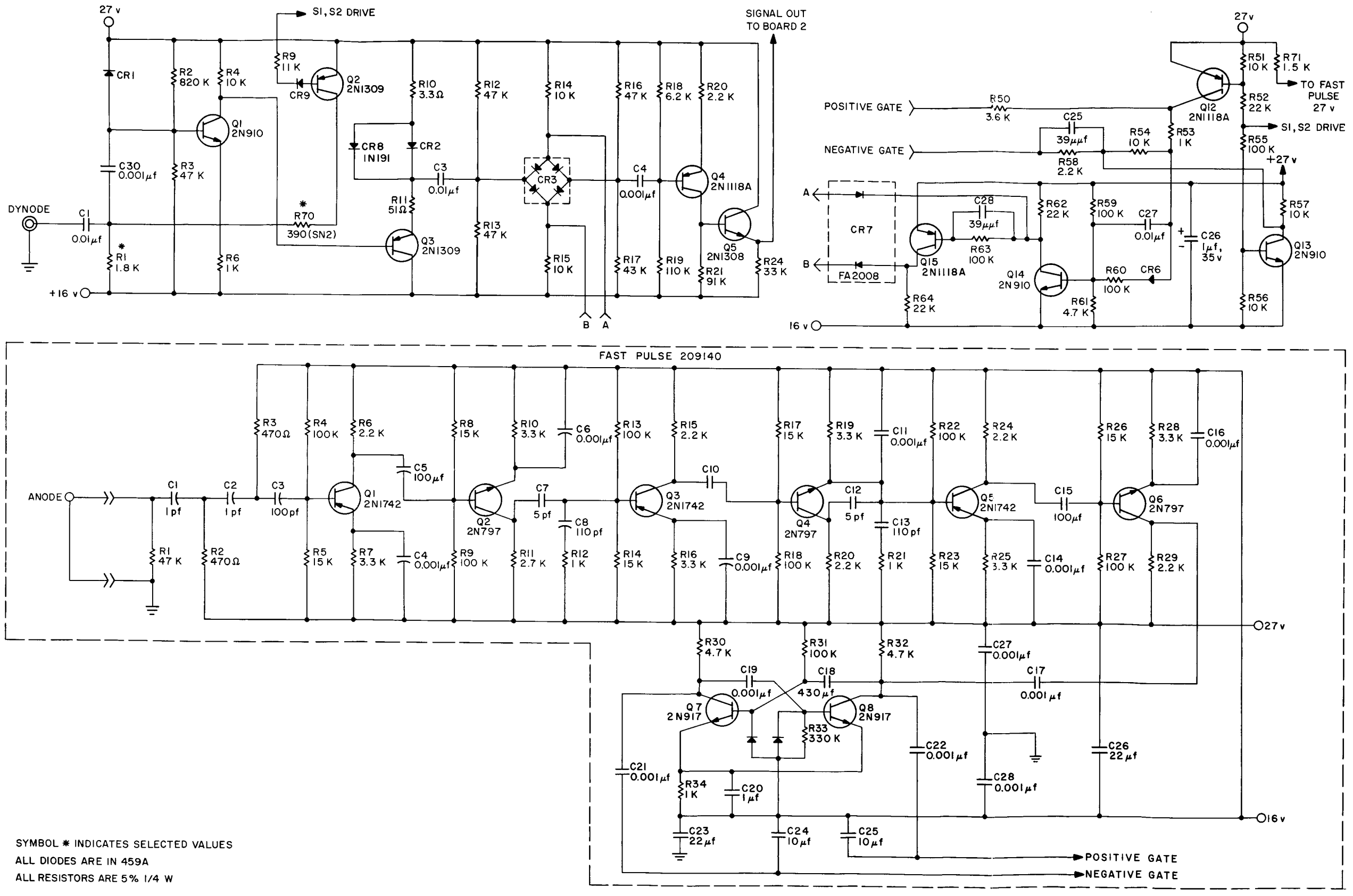


Fig. 27. Electron-proton spectrometer block diagram



SYMBOL * INDICATES SELECTED VALUES
ALL DIODES ARE IN 459A
ALL RESISTORS ARE 5% 1/4 W

Fig. 28. Electron-proton spectrometer decider gate schematic diagram

flip-flop Q14 and Q15, which provides a low impedance path across diode bank CR3 when protons are present. When it is desired to count protons, the gate is operated normally closed and is opened by outputs from the fast amplifier to emit protons. This is accomplished by the reverse action of that which occurred in the electron mode.

The proton threshold is set at about 550-kev energy loss in the scintillator. The minimum-energy proton has an energy of about 950 kev before passing through the two light-shielding aluminized foils (1 mg/cm^2). It is stopped in a plastic scintillator and does not enter the cesium iodide crystal. In the electron mode, protons which lose less than 550 kev of energy in the crystals are treated as electrons, since they do not close the gate. Consequently, the lowest-energy electron which can be allowed into the system is the one whose last dynode pulse height corresponds to that of a 550-kev proton. An electron which loses 70 kev in the crystal will have an energy of approximately 80 kev before entering the light-shielding foils. These electrons pass through the plastic scintillator and enter the cesium iodide crystal.

The highest-energy electron which can be analyzed is the one just below the region of pulse height ambiguity which occurs at 800 kev. The highest energy proton which can be analyzed is the one which pushes the region of ambiguity to sufficiently high energy ranges, at which few protons are expected to be encountered. For an upper energy choice of 5 mev, the ambiguity occurs above 40 mev.

The output of transistor Q5 of the decider gate in Fig. 28 is directly coupled to the input of the pulse shaping circuitry shown in Fig. 29. The circuitry shown in Fig. 29 provides nonlinear range compressing amplification to the input pulses to permit covering the wide range of pulse heights in the proton mode. The great range for protons originates in the fact that low-energy protons lose most of their energy in the relatively low-efficiency plastic scintillator, while high-energy protons lose most of their energy in the relatively high-efficiency cesium iodide crystal.

After amplification by a pulse shaper in Fig. 29, the pulses are sorted by a low-power, 8-channel differential analyzer shown in Fig. 30. Channels 1 through 7 register the number of pulses in fixed energy bands by biasing transistors Q1 through Q7. The energy ranges covered are 80 to 800 kev for electrons and 950 kev to 5 mev for protons. The 8th channel is an overflow channel in which all electrons are counted above 800 kev and protons between 5 and 40 mev. Protons above 40 mev will add to the counts in the first 7 channels, but it is expected that the number of such high-energy protons will be very small. The voltage drop across the diode string shown to the right in Fig. 30 is used for biasing the input transistors of the differential analyzer.

The standardized pulses from transistors Q18 through Q25 in Fig. 30 are then used to charge capacitors C1 through C8 through diodes CR1 through CR8 shown in Fig. 31. The diode is especially selected to have a logarithmic voltage current characteristic over 7 current decades and a very high back resistance. Analysis shows that this circuit constitutes an information storage system in which the voltage on the capacitor is proportional to the logarithm of the number of counts received from about 10 to 10^5 counts and is easily calibrated down to 1 count. This type of analog storage serves as an efficient data reduction system since the logarithmic characteristic provides a constant percentage uncertainty in the number of counts if the voltage is read out with a constant uncertainty in voltage. The storage system is designed to preserve information for the 40-sec period between readouts. The storage time is limited by the leakage through the charging diodes. The present system operates the temperatures up to 125°F before serious leakage occurs.

After each readout, the DAS generates a sequence pulse to the trigger amplifier and 10-millisec multivibrator shown in Fig. 32. The multivibrator output sets the state of flip-flops 1 through 4. These in turn are sampled by the tunnel diode *and* gates, which include CR29 through CR38. The output of the tunnel diode *and* gates is used to activate the magnetic read switch drivers Q1 through Q11, shown in Fig. 31. When the driver is indirectly turned on by a sequence pulse, a particular magnetic read is switched to sample the storage capacitor. This output is presented to the amplifier and buffer circuitry consisting of V1 and Q12 through Q15, where it is signal-conditioned and displayed to the DAS. The ninth position provides calibration dc levels for the electrometer amplifier, while a tenth alternately provides a temperature measurement of the detector and electronics. After each storage capacitor is read out, it is immediately dumped by means of an 11th magnetic read switch.

The power required by the electron-proton spectrometer experiment is provided by the scientific TR unit. The dc voltage is regulated at 28 v, ±3%.

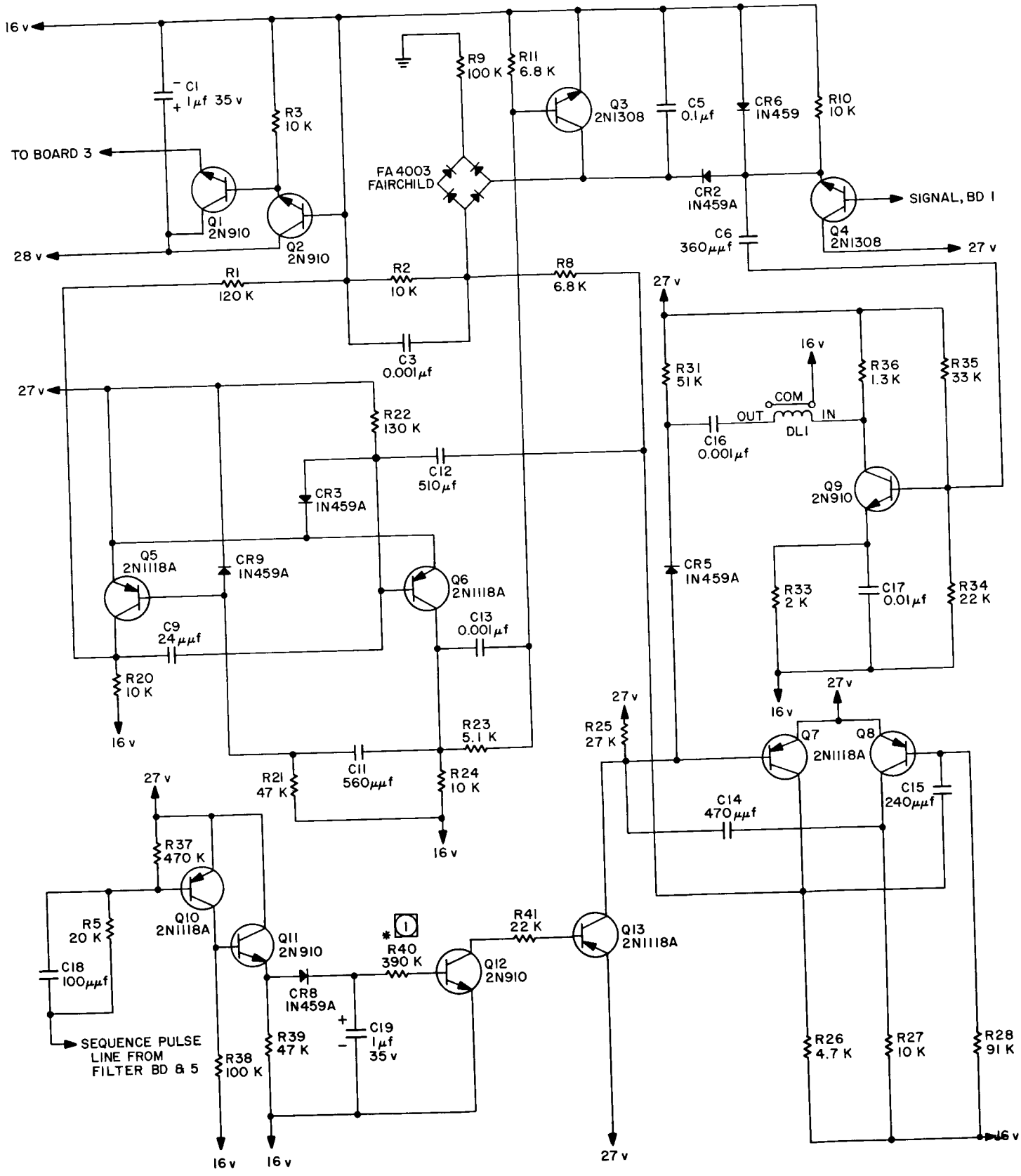


Fig. 29. Electron-proton spectrometer pulse shaper schematic diagram

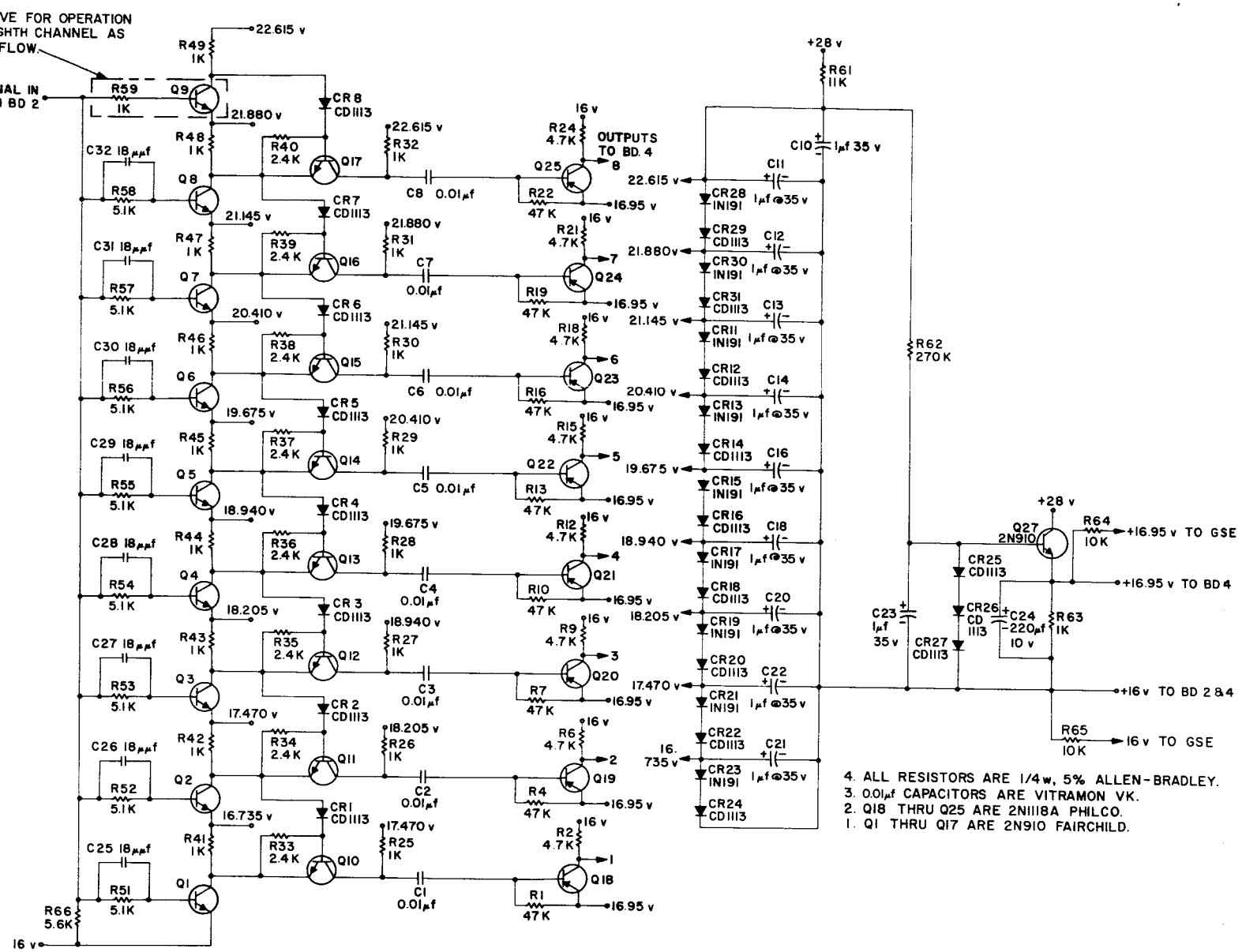
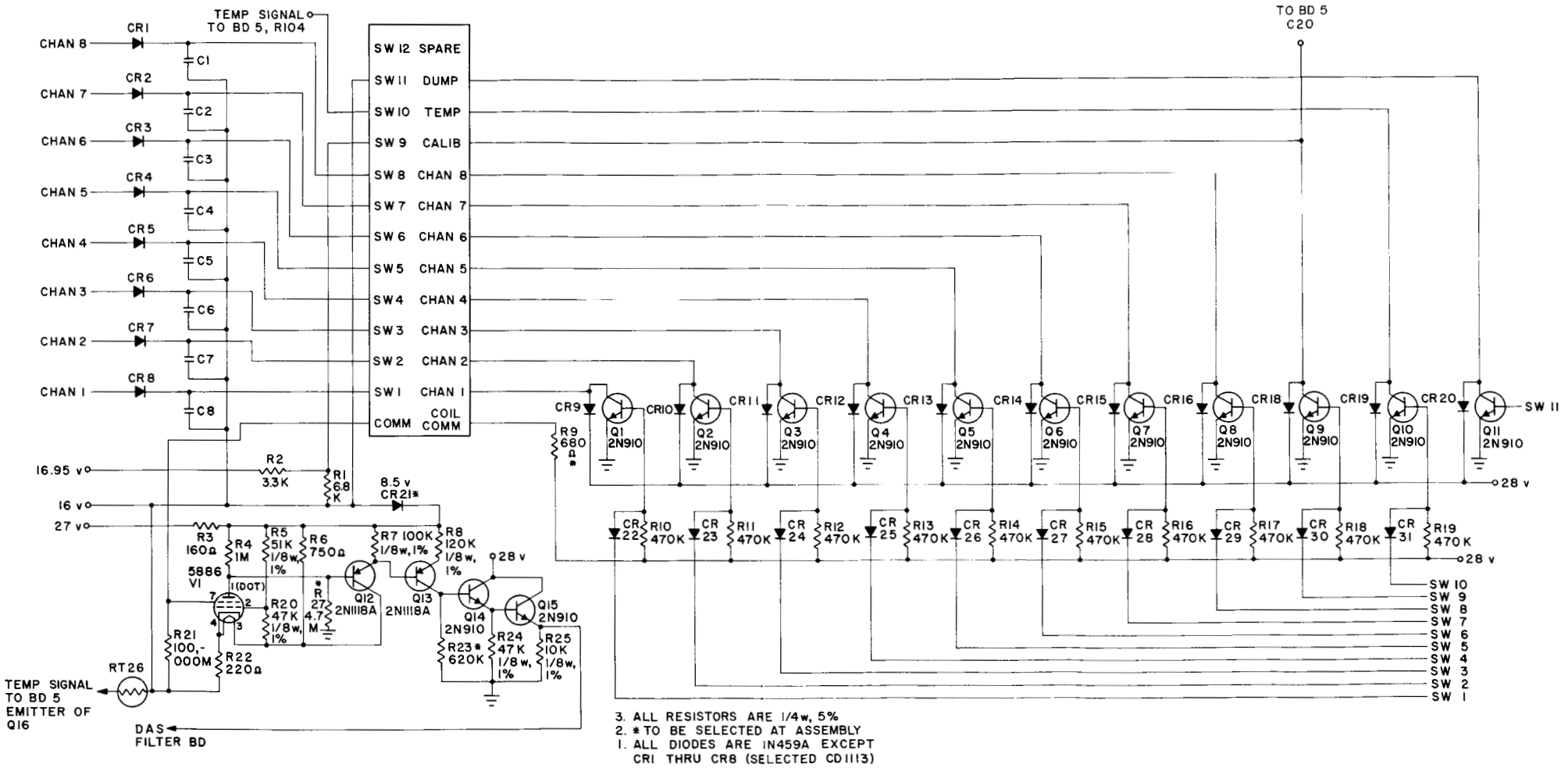
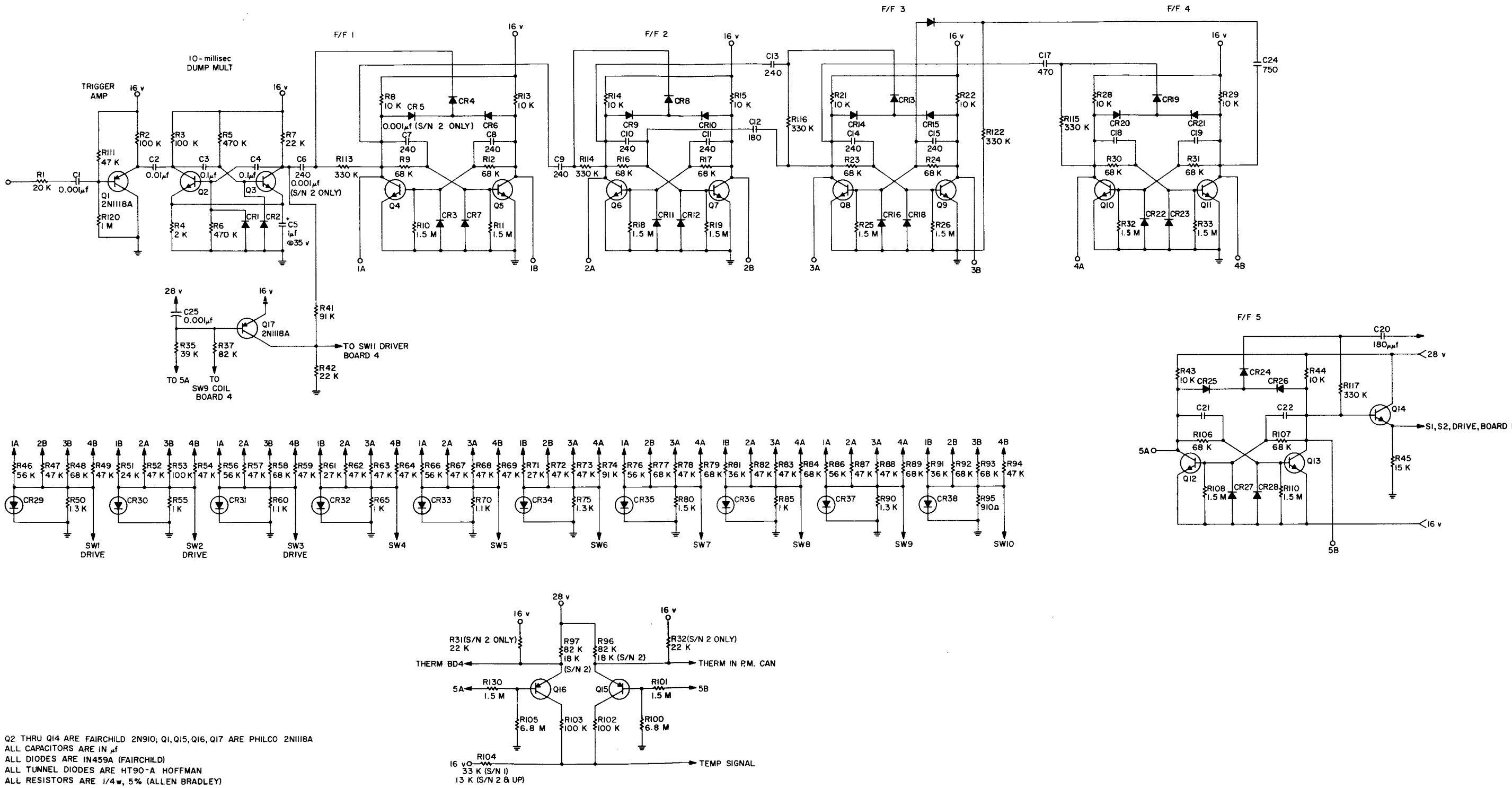


Fig. 30. Electron-proton spectrometer pulse height analyzer schematic diagram



3. ALL RESISTORS ARE 1/4w, 5%
2. * TO BE SELECTED AT ASSEMBLY
1. ALL DIODES ARE IN459A EXCEPT CR1 THRU CR8 (SELECTED CD1113)

Fig. 31. Electron-proton spectrometer storage and readout schematic diagram



Q2 THRU Q14 ARE FAIRCHILD 2N910; Q1, Q15, Q16, Q17 ARE PHILCO 2N1118A
ALL CAPACITORS ARE IN μf
ALL DIODES ARE IN459A (FAIRCHILD)
ALL TUNNEL DIODES ARE HT90-A HOFFMAN
ALL RESISTORS ARE 1/4w, 5% (ALLEN BRADLEY)

Fig. 32. Electron-proton spectrometer timer sequencer schematic diagram

IX. IONIZATION CHAMBER EXPERIMENT

The ion chamber, which was designed to measure the amount of ionization radiation in space between the Earth and Moon, consists of three subassemblies: a stainless-steel sphere, an electrometer, and a preamplifier subassembly. The 5-in.-diameter sphere is pressurized to four atmospheres with argon and inert gas. The electrometer consists of a quartz stem collector and a fine fiber element separated from it. The preamplifier electronic package includes a three-stage transistor amplifier. An ion pair is created in the gas within the chamber whenever ionization radiation separates an electron from its nucleus. When the collector electrode collects a specific potential with respect to the fiber electrode, it is recharged and simultaneously produces a voltage pulse across the load resistor. Figures 33 and 34 are, respectively, a photograph and a block diagram of the ionization chamber experiment.

A. Description of the Ionization Chamber

The electrometer consists of a collector and fiber in the chamber's spherical shell, as shown in Fig. 35. The collector is a tapered rod of fused quartz coated with aquadag. This rod collects electrons generated in the chamber gas from ionization radiations. A quartz fiber also coated with aquadag is mounted on the quartz rod and is electrically isolated from the collector by an uncoated portion of the quartz. This fiber passes over the collector and is separated from it by 0.02 in. A potential of 310 vdc is applied to this fiber through a 20,000-ohm resistor. This positive potential therefore attracts free electrons from the fiber surface to the positive terminal of the source. When the electrostatic force of attraction between the opposite charges on the fiber and collector (approximately 10^{-10} coulombs) exceeds the mechanical resistance of the quartz, the fiber is pulled to the collector

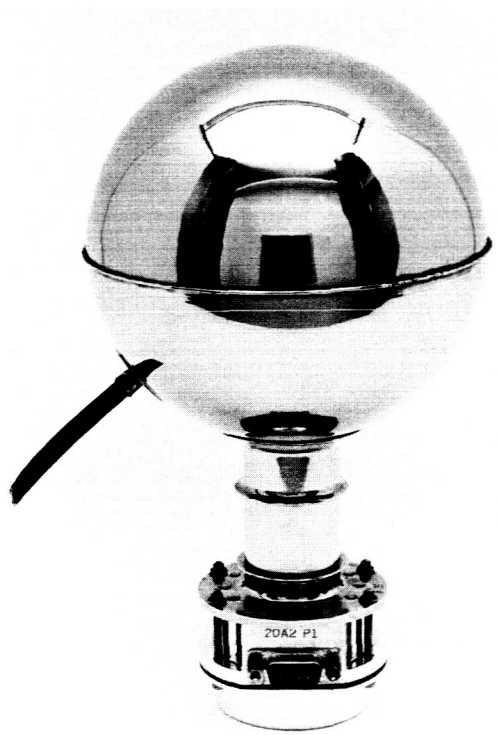


Fig. 33. Ion chamber experiment

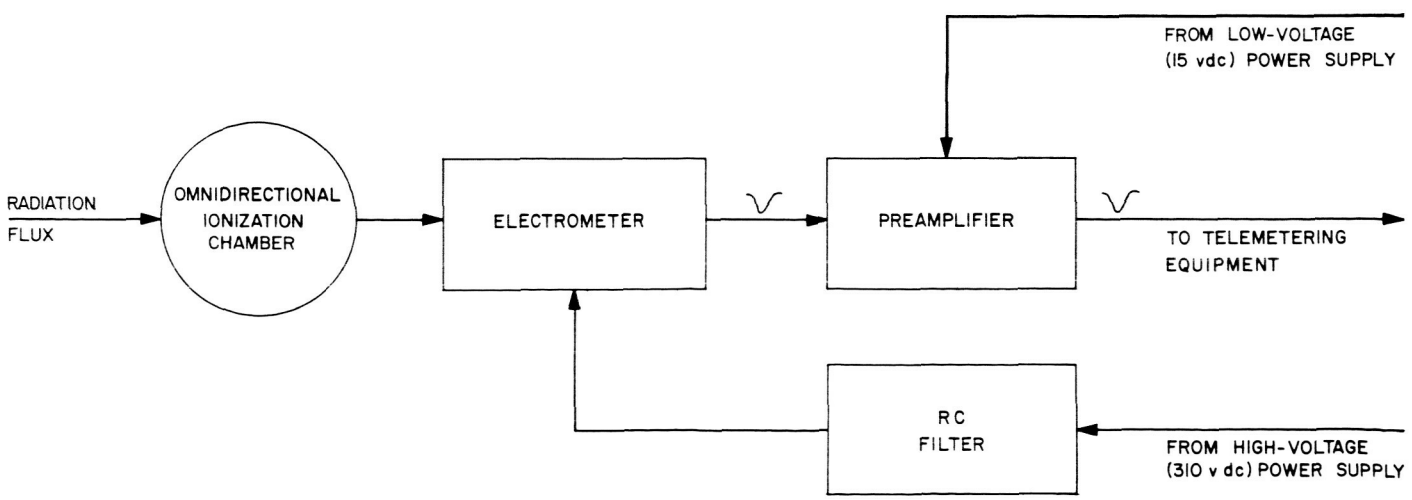


Fig. 34. Ion chamber block diagram

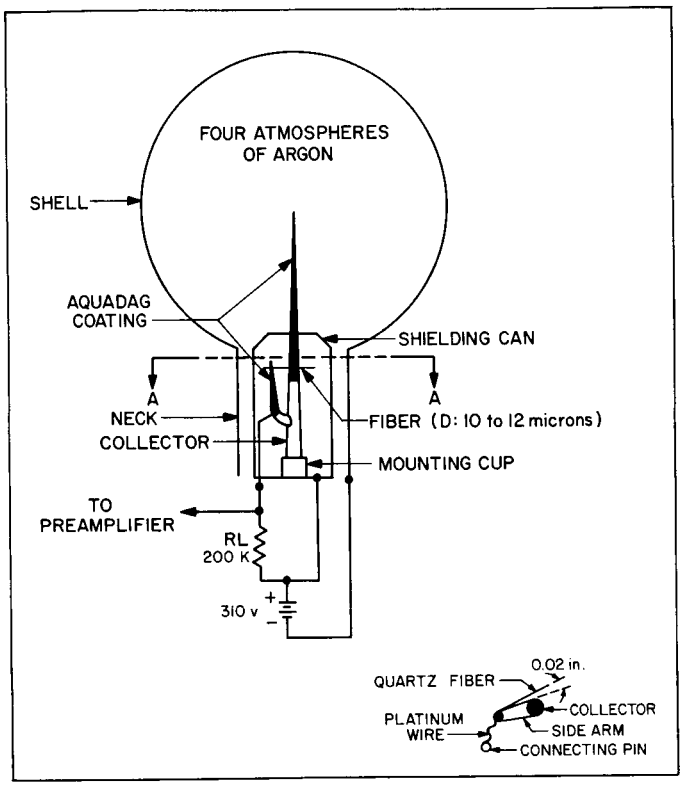


Fig. 35. Ion chamber internal mechanism

and momentarily contacts it. A surge of electrons then passes from the collector to the fiber through resistor RL to the positive source. This causes the voltage at the junction of the fiber and RL to decrease, producing a negative pulse at the input of the preamplifier. With the passage of electrons from the collector rod to the battery terminal, the charge between the rod and fiber is equalized and the fiber returns to its normal position. The useful pulse rate of this instrument is from 1 per 500,000 sec to 100 per sec, which corresponds to 1.2×10^{-2} milliroentgens per hr to 60 milliroentgens per hr. The different types of ionization radiations which can be detected by the ionization chamber are summarized in Table 2.

Table 2. Radiation types and energy penetration levels in space

Radiation type	Shell penetration energy level
Protons	≥10 Mev
Alpha particles	≥40 Mev
Beta particles	≥ 0.5 Mev
Gamma rays	Depends on energy level
Bremsstrahlung	Depends on energy level

B. The Electronics

The preamplifier schematic diagram is shown in Fig. 36. The negative pulse from the quartz integrating subassembly is routed to the base of Q1 through C1, causing the base and collector currents of Q1 to increase. The negative potential produced at the base of Q3 causes the collector current to increase, producing a negative-going pulse at the emitter of Q3 because of the increased voltage drop across R3. Resistor R2 and capacitor C3 decouple preamplifier pulses from the supply by shorting them around R2 through C3 to ground. Feedback transistor Q2 controls the dc collector current of Q1 and Q3 for static operation of the preamplifier. Since the DAS will only respond to positive pulses, an inverting amplifier has been added and located in the particle flux electronics package. The negative pulse output from the preamplifier is coupled to the base of Q4, thereby turning the inverter on and producing a postive pulse to the DAS.

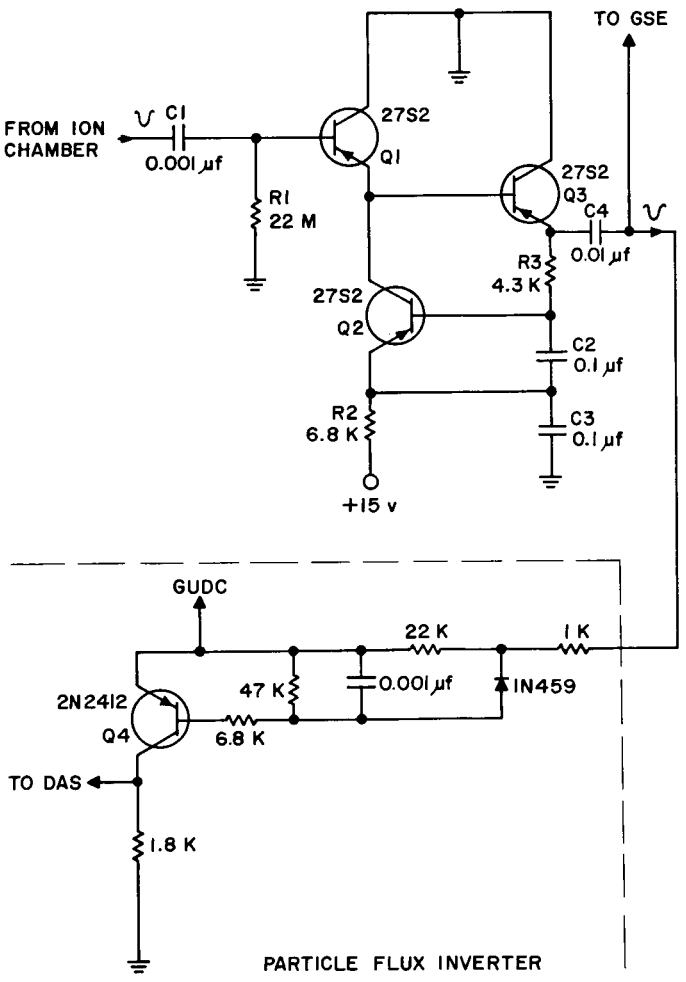


Fig. 36. Ion chamber schematic diagram

X. PARTICLE FLUX EXPERIMENT

The particle flux experiment (Fig. 37) has been designed to detect protons with energies greater than 10 mev, alphas with energies greater than 40 mev, and electrons with energies greater than 0.5 mev by direct penetration. Three Geiger-Muller tubes are used to detect particle flux. Each GM tube consists of an anode and a cathode enclosed in a mixture of neon and a halogen quenching gas. A particle passing into the tube creates an avalanche of ion pairs consisting of electrons and gas molecules from collisions with the neon. The electrons are attracted to the anode, while the positive gas molecules move towards the cathode. When a specific potential between the anode and cathode has been reached, an electrical breakdown of the gas results and produces a positive pulse across the load resistor which is connected to the cathode. The discharge is quickly quenched by the halogen gas to increase the counting rate capabilities.

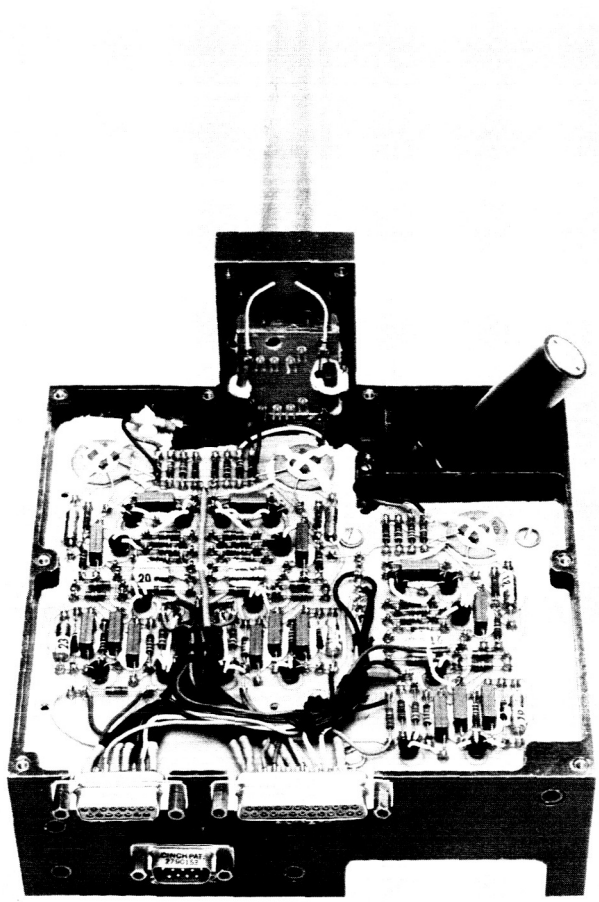


Fig. 37. Particle flux experiment

A. Description of the Geiger-Muller Counter

Figure 38 is a block diagram of the particle flux experiment. Commercial Geiger-Muller tubes in specially designed shields are used. Tubes 1 and 3 are 900-v Radiation Counter Laboratory 10311 tubes with a glass wall having a thickness of 0.030 gm per cm^2. Tube 1 is shielded by a thin stainless-steel envelope to match that of the ion chamber; tube 3 is shielded with beryllium. The counting rate of tubes 1 and 3 can vary from less than 1 per sec to 50,000 per sec. The expected rate in space is approximately 15 per sec. Tube 2 is an Anton 213 end window counter. The window, which is made of a very thin piece of mica, admits electrons with energies greater than 40 kev and protons with energies greater than 0.5 mev. A small shield defines the solid angle through which particles can reach the window. The solid angle has the shape of a cone with a half angle of 45 deg. The counting rate from this tube can vary from less than 0.01 per sec to 30,000 per sec. The expected rate in space is approximately 0.1 per sec. The coincidence rate between tubes 1 and 3 is also measured with a resolution time of 1 μsec. In order to produce a coincidence output, a particle must penetrate at least 3 walls, which requires that a proton have energies greater than 18 mev, an alpha greater than 72 mev, and an electron greater than 1.2 mev. The coincidence counting rate can vary from less than 1 per sec to 50,000 per sec. The expected rate in space is approximately 0.2 per sec.

B. The Electronics

A schematic diagram of the stainless-steel or beryllium Geiger tube amplifier and pulse shaper is given in Fig. 39. Also included is the coincidence gate and amplifier for the beryllium and stainless-steel outputs. The circuitry for all three Geiger tubes is identical, the only difference being the bias voltage supplied to the tubes. The positive pulses from the counter are coupled directly to the amplifier's input stage emitter follower, which presents a high impedance to the detector. The output of the emitter follower is direct-coupled to the base of the second stage, a common emitter phase inverter which in turn drives the complementary output stage. The output of all three counters is presented to the DAS, while the stainless steel and beryllium outputs are also injected into the bridge network of the coincidence amplifier. If neither the beryllium nor the stainless-steel pulse occurs,

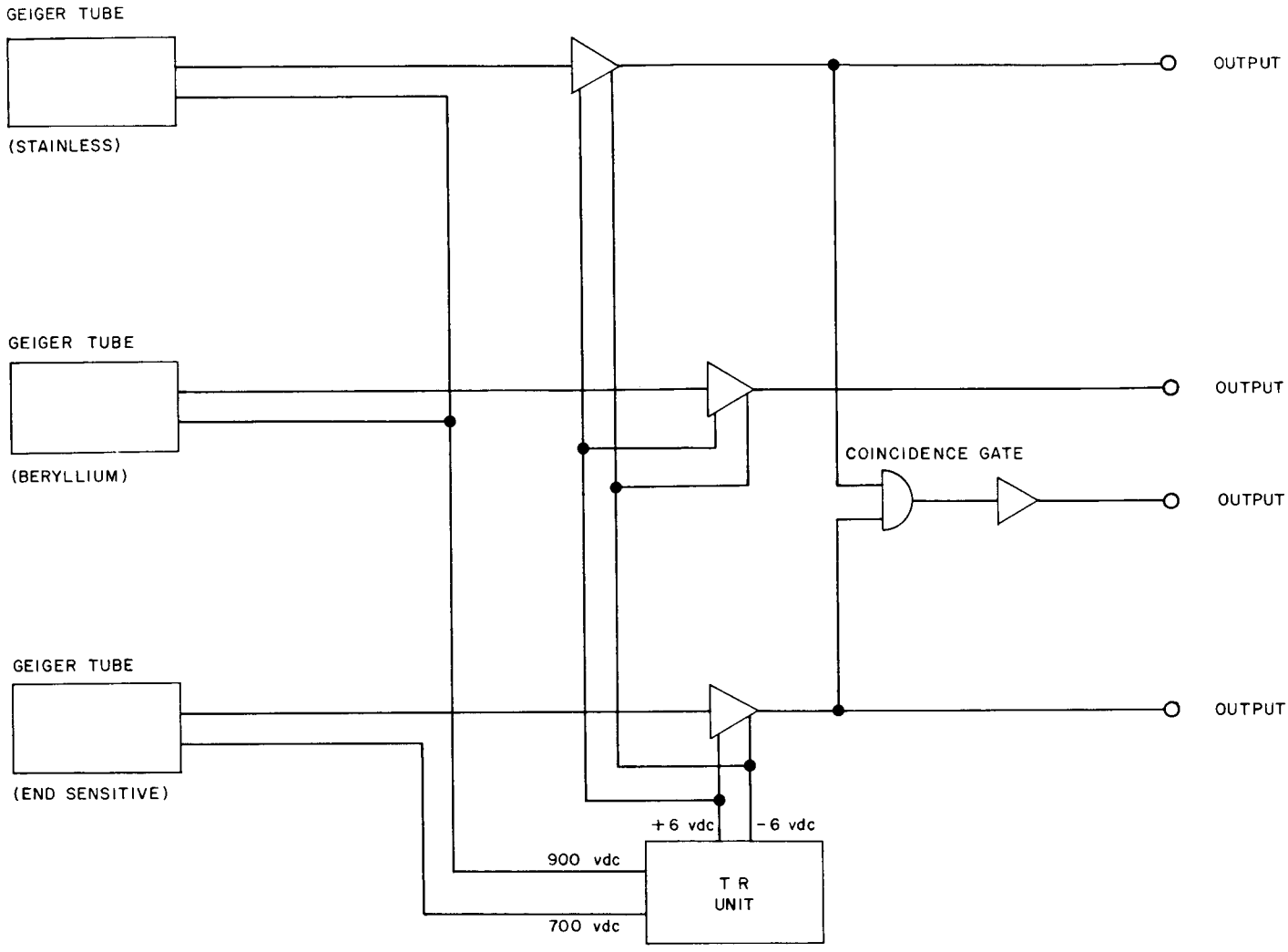


Fig. 38. Particle flux experiment block diagram

the emitter collector junction of Q21 and Q22 will remain positive, holding Q22 off. When a pulse is present from both beryllium and stainless-steel outputs, CR5 and CR6 are reversed-biased, allowing inverter Q22 to be turned on. The output from Q22 is coupled to the base of inverting amplifier Q23, which turns Q23 on. The output of Q23 then drives the complementary output stage, which feeds the DAS.

C. *The Power Supply*

A single power supply provides the dc voltages required to operate the ionization chamber and the particle flux experiment. The power supply is an ac to dc converter. The input is a 52-v, peak-to-peak square wave, and the outputs are shown in Table 3.

Table 3. Ion chamber and particle flux

Output voltage, vdc	Function
+900	High-voltage supply for the stainless-steel shielded counter
+700	High-voltage supply for the end-sensitive counter
+900	High-voltage supply for the beryllium shielded counter
+310	High-voltage supply for the ion chamber
+ 15	Voltage supply for the ion chamber electronics
− 6	Voltage supply for the particle flux electronics
+ 6	Voltage supply for the particle flux electronics

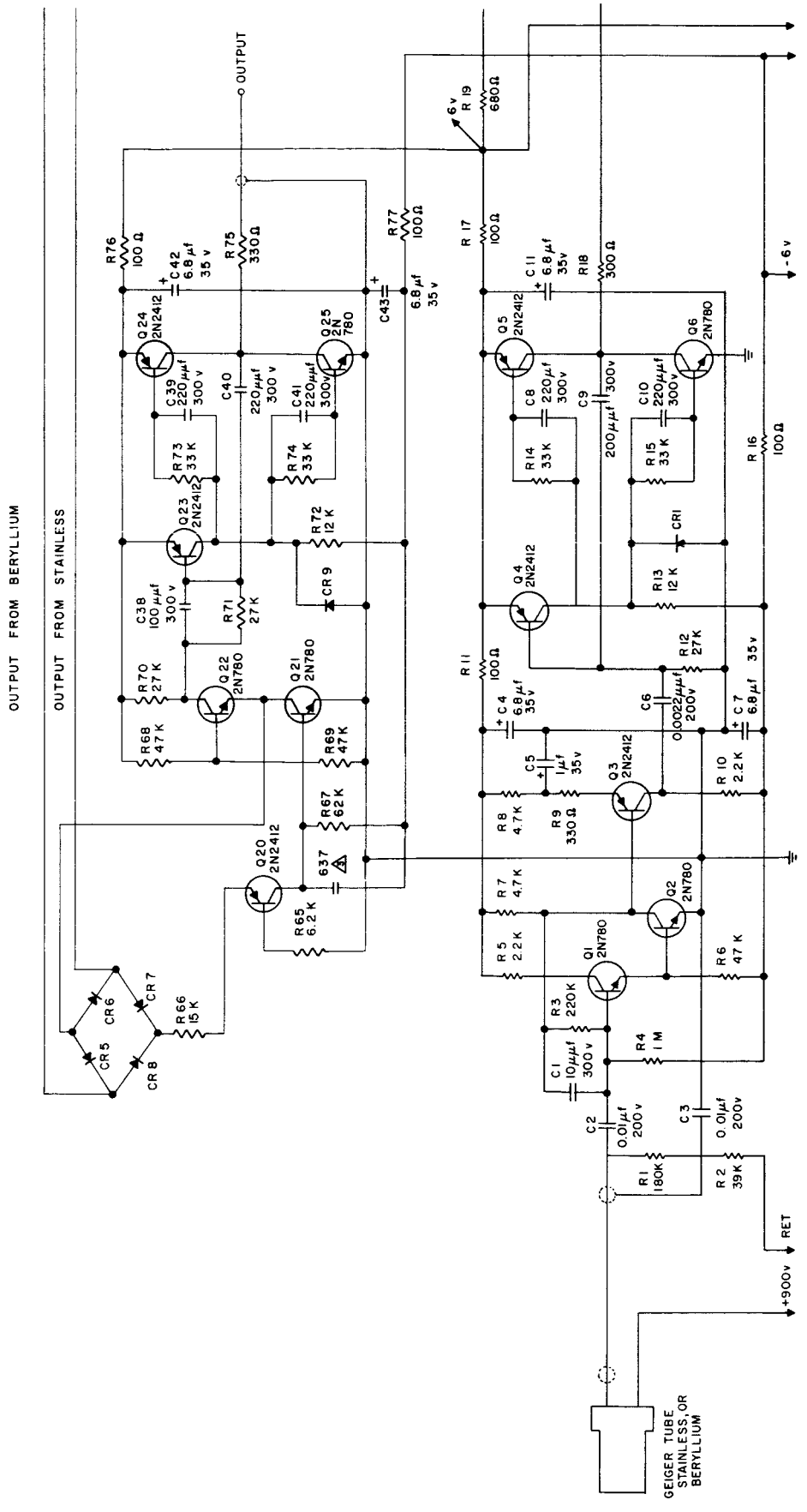


Fig. 39. Particle flux experiment schematic diagram

XI. SEARCH COIL MAGNETOMETER EXPERIMENT

At present, very little is known about the flow of the solar wind with its imbedded magnetic fields past the Moon. It is difficult to predict whether there will be a low shock wave as the solar wind flows past the Moon or what the properties of such a shock wave would be, but it is felt that there may be turbulence and hydromagnetic waves associated with the shock front. The standoff distance of shock as well as the location and structure of the turbulence and waves depends on the magnitude of the intrinsic lunar field. The search coil magnetometer was specifically designed to measure these magnetic field fluctuations in the frequency range from 1 to 1000 cps. The results of the experiment when correlated with the plasma measurements should provide significant new information about the dynamics of the solar plasma: that is, the properties of its flow past a large obstacle as well as the characteristics of its instabilities. A signal detected by the search coil magnetometer is analyzed into Fourier components by a spectrum analyzer consisting of five wideband tuned amplifiers. The center frequencies of these amplifiers are at 3.2, 10, 32, 100, and 320 cps. The rms voltages developed in each channel are rectified and stored as dc voltages at the output points. The search coil magnetometer consists of two packages: the sensor and electronics packages shown in Fig. 40. The sensor package contains the search coil assembly and a low-noise preamplifier. It is filled with styrofoam to immobilize the electronics and provide good thermal insulation. This package also contains a heater with the associated temperature-control circuit. The electronics package contains the main amplifier with automatic scale switching, the spectrum analyzer, and an inflight calibration circuit.

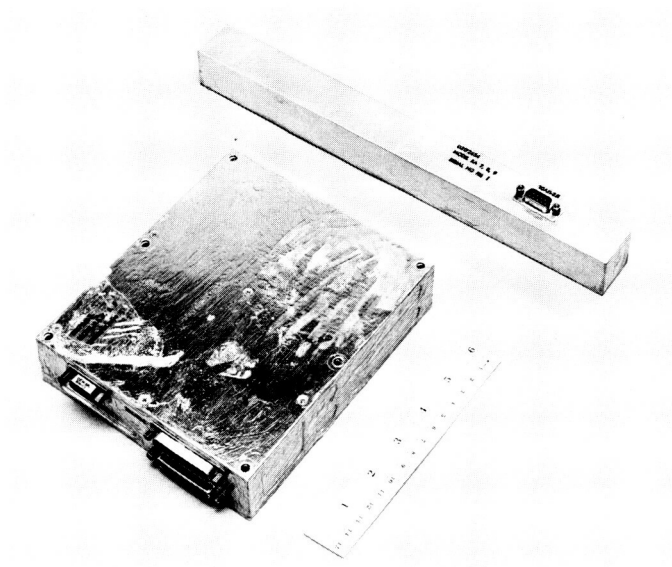


Fig. 40. Magnetometer experiment

A. The Sensor

Magnetic field fluctuations are converted to voltages by the search coil sensor, which consists of 100,000 turns of No. 50 teflon insulated wire wound on eight bobbins, each 1 in. long and mounted on a laminated core of four mill strips of orthonal. The search coil scale factor is approximately 7 μv sec per gamma of magnetic flux.

In order to facilitate measurements of low-level fluctuations, particularly at low frequencies, a low-noise preamplifier is included in the same assembly with the search coil. This preamplifier utilizes a field effect transistor in the first stage in order to present a high impedance to the coil output, which has about 80,000 ohms in series with 800 henries of inductance. The preamplifier also includes a differential amplifier and an emitter follower output stage, both utilizing low-noise transistors. The gain of the preamplifier, which includes approximately 20 db of negative feedback, is 100 at midfrequencies. A typical frequency response curve is shown in Fig. 41. The peak above the theoretical 6-db/octave slope is due to the resonance of the core, while the dip at about 450 cps is due to the necessary compensation network in the amplifier.

B. The Electronics

A brief functional description of the search coil magnetometer electronics is presented using the schematic diagrams in Fig. 42ab and the block diagram in Fig. 43. In Fig. 43 the preamplifier output is further amplified in the main assembly by two feedback amplifiers separated by a switch attenuator. The first of these amplifiers has a gain of approximately 7; the second has a gain of 40. The output of the first amplifier also controls the attenuation scale through the use of the amplifier and comparator circuitry. The output of the second amplifier is applied to 5 spectrum channels tuned as shown in Fig.

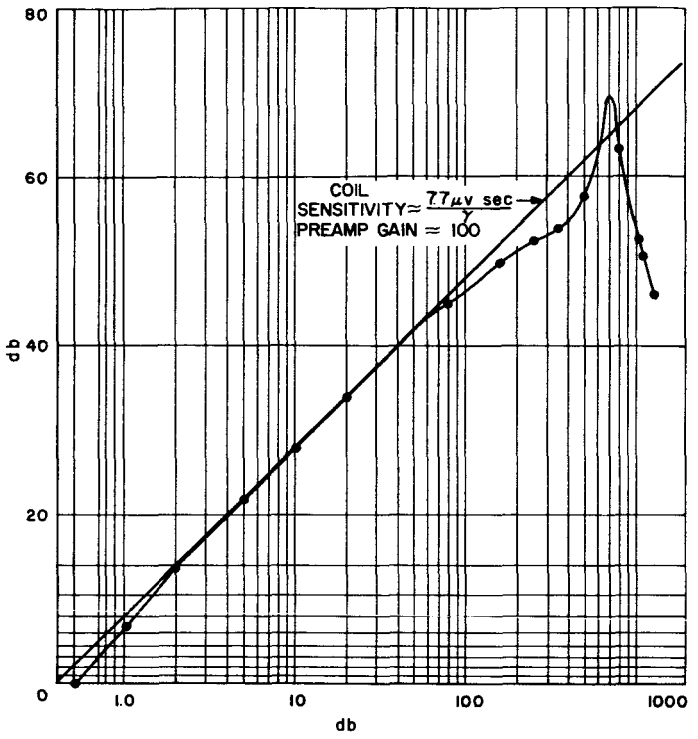


Fig. 41. Magnetometer probe response curve

43. Each spectrum channel contains a band-pass amplifier utilizing a bridged-T network in the feedback path of a differential amplifier. The output of this amplifier, which has a Q of approximately 3, is converted to dc by a peak-to-peak detector and a long-time constant filter. The gain at center frequency of the spectrum channels is 13 vdc per 1-v rms. The outputs of the filters are transmitted to the DAS through the use of emitter follower output stages. IFC on and off commands in the DAS control the state of the IFC flip-flop which turns the IFC squarewave generator on or off. This squarewave signal is then routed to the preamplifier for an in-flight calibration of the magnetometer.

Signal flow from the preamplifier will be demonstrated using the schematic in Fig. 42b. The input is ac-coupled to the base of the differential amplifier Q201, which is biased at approximately 7 volts. The output of Q201 is directly coupled to amplifier Q202, which provides unity dc feedback to Q201 for bias stability, and input to the scale switching differential amplifier Q210 and Q211 and an output to the attenuator circuitry. If it is assumed that the output from the scale switching differential amplifier is not great enough to turn on Q213, the following condition will be true: the biasing of Q204 is such that there is a high base-to-collector and base-to-emitter resistance. This resistance, in combination with R276, R277, and R246, provides a signal attenuation of 1.3 to 1. If, on the other hand, the amplified signal does turn on Q213, Q214 is turned off, allowing the base of Q204 to go more positive, which drives Q204 closer to saturation. Effectively, the collector-to-ground resistance of Q204 is now much lower. This increases the attenuation factor to 39 to 1. The signal is again ac-coupled and amplified by Q203 and Q205. The output of Q205 is coupled to 5 bandpass amplifiers, a typical one consisting of Q206, Q207, and Q208. They are very similar to the voltage amplifiers previously described, except that each contains a bridge-T network in the feedback path (C205, C206, R221, and R222) and a broadly tuned RC network (C202, R216, C204, and R218 and R217 in parallel) in the input. By proper choice of components, the bandpass amplifiers have an overall gain of 5.5 at center frequency and a circuit Q of approximately 3. Each bandpass amplifier output is ac-coupled to a peak-to-peak detector filter and emitter follower typified by CR204, CR205, C207, and Q209. A temperature-compensated bias supply for all detectors is provided by RT101, RT102, and R142.

With the magnetometer in the most sensitive mode—or with the input signal at a low level and Q204 not conducting—the scale output transistor Q221 is also not conducting owing to the attenuated voltage on the base caused by the conduction of Q214. In this condition the scale output is approximately 0.5 volts. Zener diode CR210 is not broken down because of the voltage divider action of Q214; therefore, Q216 is held off and the IFC attenuator Q215 is turned on. The IFC signal from flip-flop Q219 and Q220 is attenuated by R248, R250, and a low resistance between the collector and ground of Q215. This ensures that the IFC signal will not drive the amplifier into its low sensitivity range. When the magnetometer is in the low sensitivity mode, Q214 is turned off and enough base current is provided to turn on Q221. The output scale indication would now be approximately 3 volts. In low sensitivity, zener diode CR210 breaks down, Q216 conducts, and the IFC attenuator Q215 is turned off. The IFC signal from the flip-flop is now only slightly attenuated by the action of Q215.

The IFC signal is generated by the unijunction transistor Q222, which oscillates at 10 cps during the time that the flip-flop consisting of Q217 and Q218 is in the proper state. The input to Q217 is the IFC-off pulse which occurs approximately once every 5 min, and the input to Q218 is the IFC-on pulse which occurs approximately once every 172 min. Both of these commands are

given by the DAS. Since an off pulse occurs simultaneously with every on pulse, different input time constants controlled by capacitors C210 and C220 are utilized to assure priority to the on pulse. The differentiated IFC-on pulse turns off Q218, allowing the proper bias to be applied to the emitter of Q222 for an oscillator condition to be fulfilled. The output of the oscillator is coupled to flip-flop Q219 and Q220, which divides the signal to 5 cps and produces a symmetrical squarewave output. The output is then fed to the IFC attenuator circuit, which has been previously discussed.

C. The Power Supply

The input 2400-cycle power is transformer-coupled to two full-wave rectifiers. The high-voltage winding has approximately 26-v rms on each side of its center tap. The low-voltage winding is utilized to enable more efficient operation of the voltage regulator. In order to limit turn-on surges to approximately 50% greater than the nominal load, Q1, C2, and R2 are utilized as a current limiter. The remaining circuitry Q2 through Q5 comprises a voltage regulator giving approximately 0.1% over-all regulation.

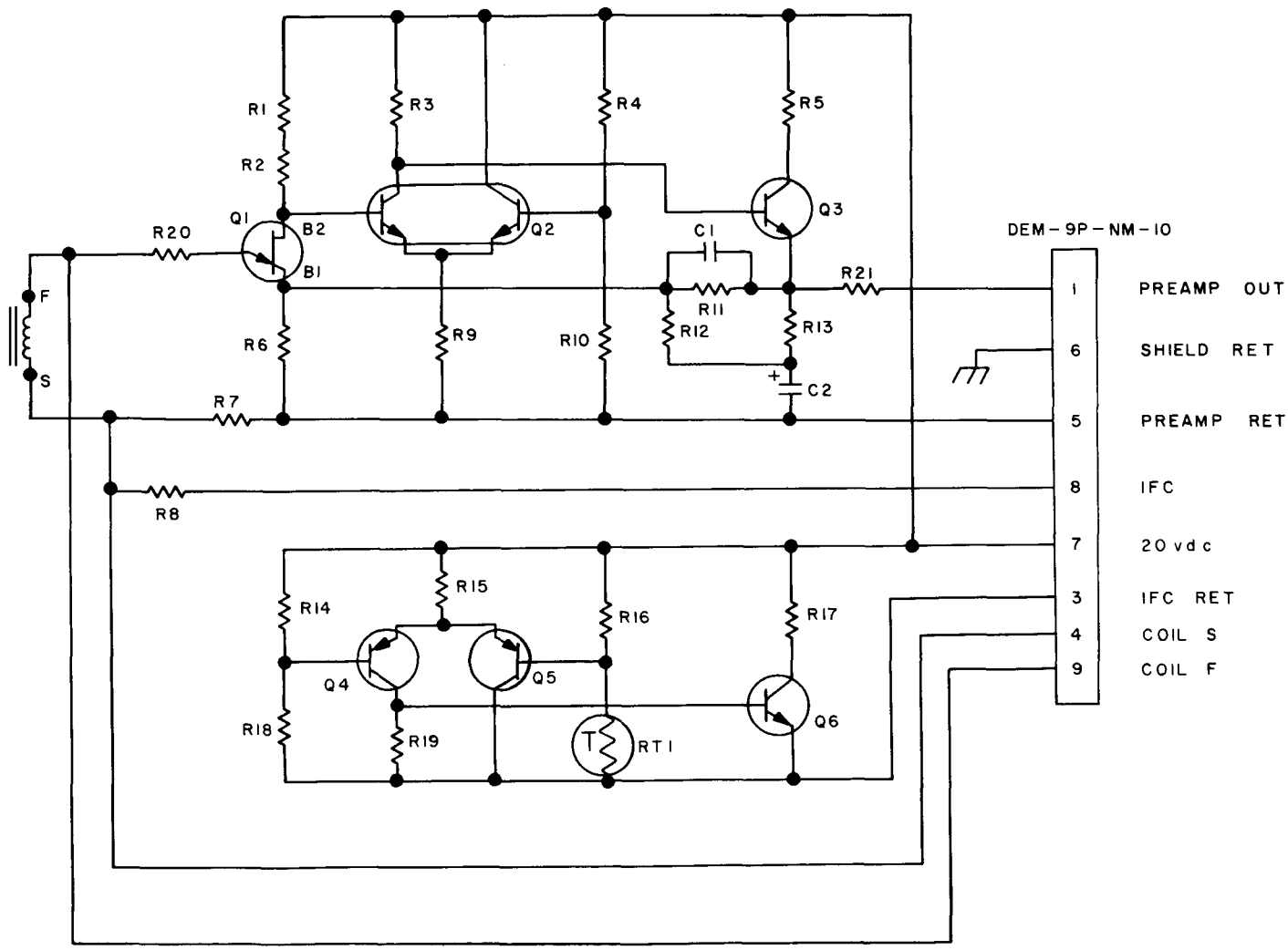


Fig. 42a. Magnetometer schematic diagram

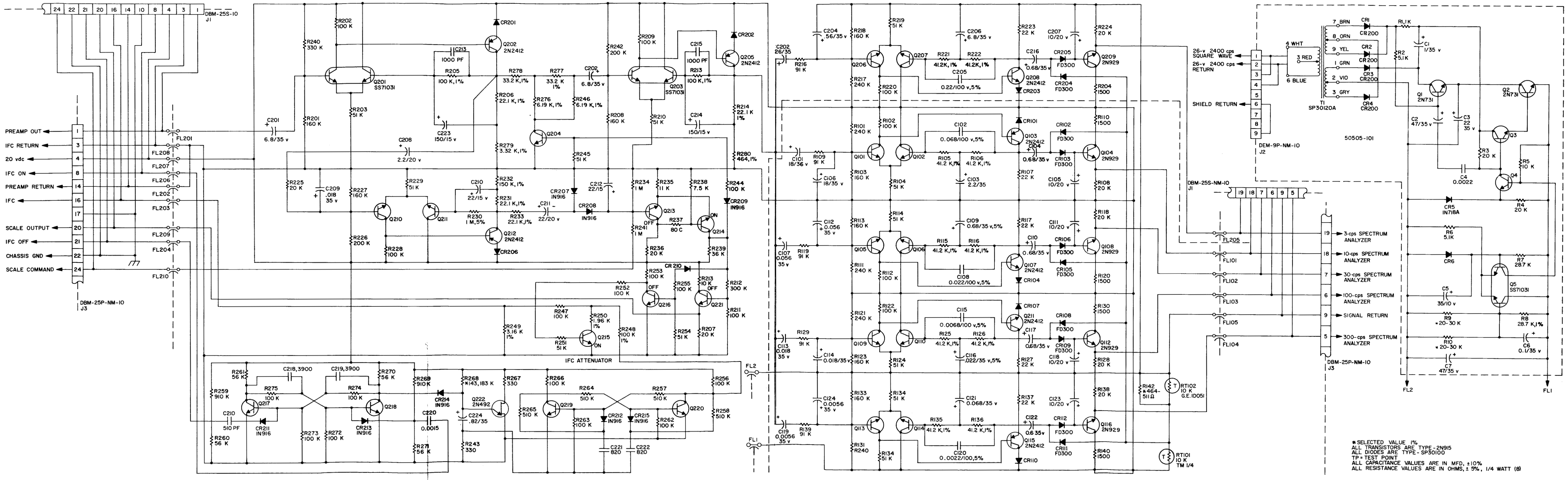


Fig. 42b. Magnetometer schematic diagram

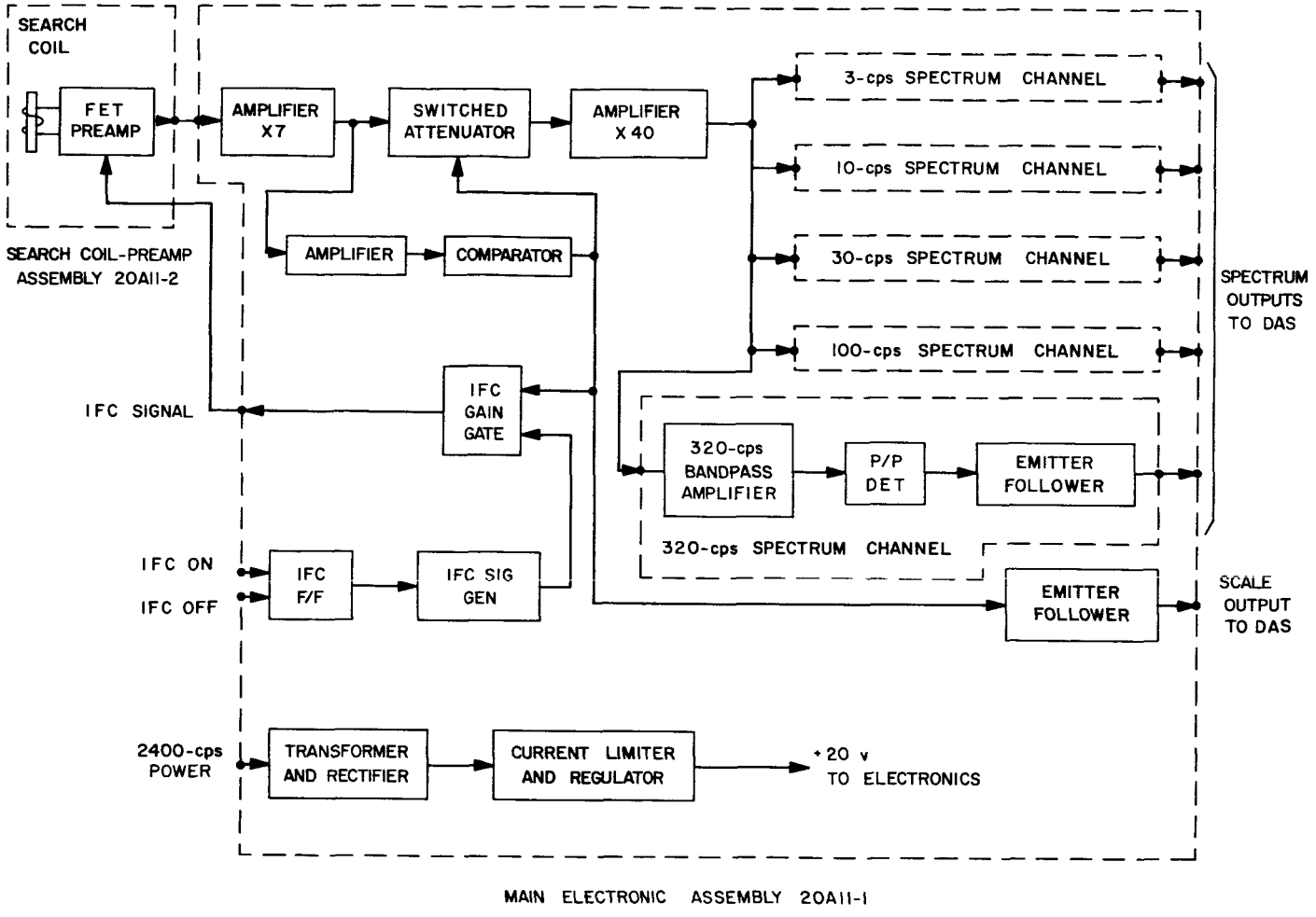


Fig. 43. Magnetometer block diagram

XII. LOW-ENERGY ION DETECTOR EXPERIMENT

The low-energy ion detector experiment is designed to measure the number density and energy of positively charged particles with energies up to 30 ev. The experimental technique is similar to the positive ion retarding potential experiment flown successfully on the *Explorer 8* satellite.

In the Van Allen radiation belts, the experiment will measure the total proton flux and the relative contributions of protons with energies below and above 30 ev. In cislunar space, the experiment will measure the density of the interplanetary plasma in the range of approximately 10 to 5000 positive ions per cm^3. The determination of particle density is dependent upon the ratio of vehicle to ion thermo velocity. Since the experiment is directed away from the Sun during transit, solar wind particles should not influence the measurement.

During the terminal stages of the mission, the experiment is oriented along the direction of motion of the vehicle, and measurements of the charged particle density of the lunar ionosphere will be made. By means of a retarding potential analysis, the ion detector will determine the ion species in the lunar ionosphere as the predominant constituent changes from the interplanetary plasma protons to possible heavier constituents such as HE+, 0+ and N_2+.

The sensing device for the low-energy ion detector is an ion trap consisting of three electrodes, two grids, and a solid collector (see the block diagram in Fig. 44). Particles received by the collector are amplified by the electrometer amplifier, presented to the output chopper as a dc level where an ac signal superimposed on the dc is rectified, and displayed to the DAS as an analog voltage. Bias potentials for the first grid and electrometer amplifier reference common potential are selected by a mechanical programmer which is actuated by trigger pulses from the DAS. Figure 45 is a photograph of the low-energy ion detector experiment.

A. The Sensor

The circular electrodes of the low-energy ion sensor are mounted in planar parallel geometry, with an interelectrode spacing of about 5 mm. The grids consist of gold-plated mesh of 1-mil tungsten wire. The aperture grid is the outermost grid of the ion trap, consisting of a 1.6-in. opening in a 3.5-in. guard ring mounted on a 5- by 7-in. ground plate. It is necessary to maintain the aperture grid and guard ring at negative potentials for collection of low-energy ions to overcome the positive potential of the spacecraft, which is caused by the predominance of photo emission current over the negative current due to diffusion of thermoelectrons to the space-

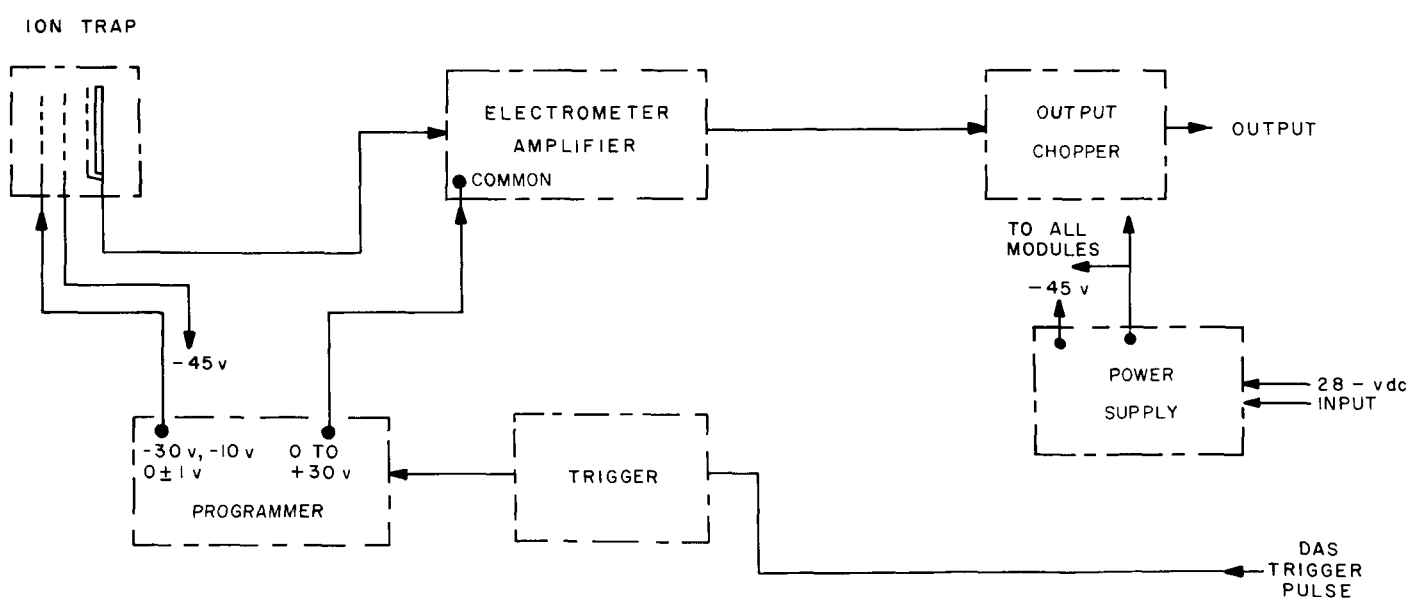


Fig. 44. Low-energy ion detector block diagram

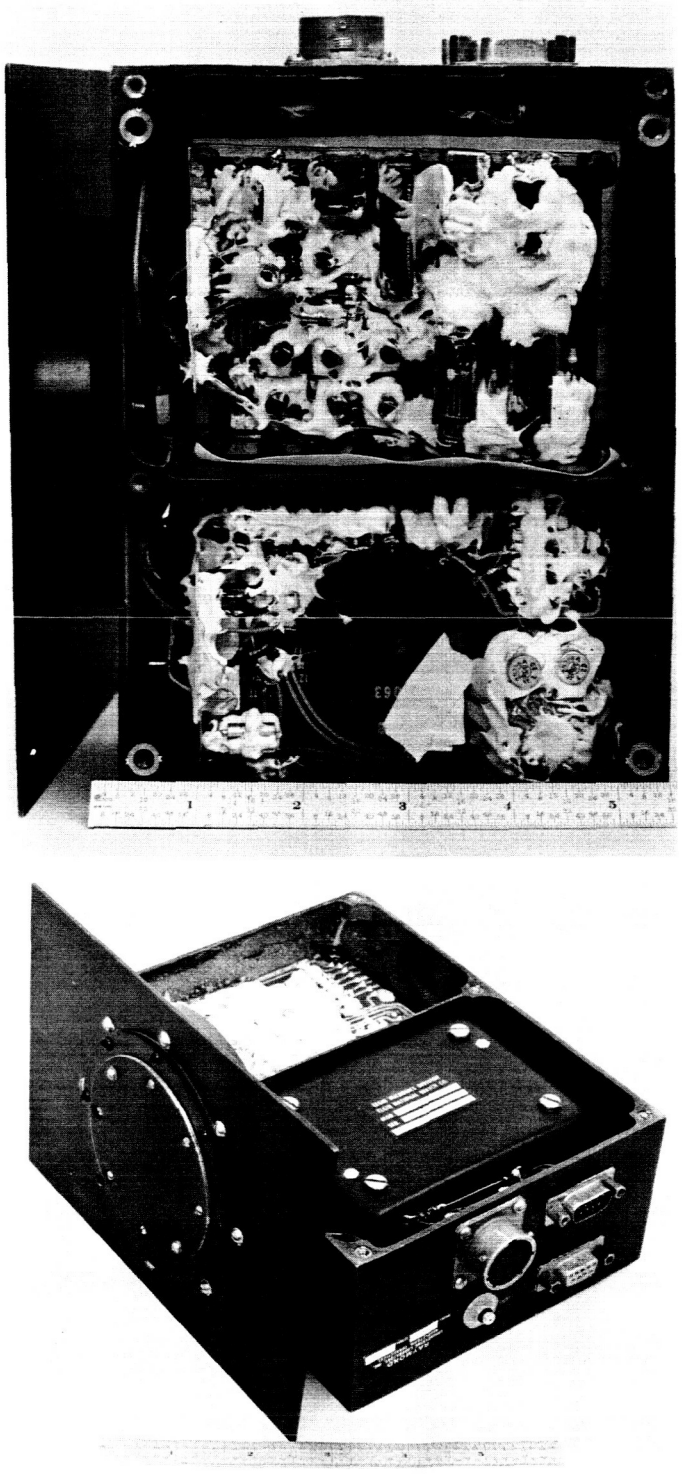


Fig. 45. Low-energy ion detector experiment

craft. A negative potential is applied to the aperture and guard during certain modes of operation, since it is estimated that a potential of about 10 v could be obtained by the spacecraft.

The second electrode of the ion trap is a 2-in. grid which is maintained at a constant potential of −45 v and serves to remove incoming low-energy electrons from the measured collector current. It also suppresses photo and secondary emission currents from the collector. Photo emission currents, if not suppressed, are considerably larger than the expected thermo-ion currents in the upper ionosphere and interplanetary plasma. The collector is a 2-in. circular plate operated in retarded and nonretarded ion collection modes. For the nonretarded modes, the collector is maintained at the same potential as the aperture and the guard ring. The low-energy ion detector is operated in retarding potential modes in order to obtain ion velocity distribution information. For these modes, a stopping potential of ten 3-v steps, a total of 30 v, is superimposed on the collector bias voltage. As the potential on the collector increases, the ions are slowed down, and those that have a kinetic energy relative to the spacecraft, less than the potential energy of the collector with respect to the plasma, are turned back. Consequently, the measured ion current is a function both of the retarding potential and of the relative velocity between the ions and the spacecraft.

B. The Electronics

Ion current from the collector is coupled to a balanced pair of 5886 electrometer tubes which have 100% feedback to maintain the input at amplifier common potential, and therefore no voltage drop is realized across the input resistor (see Fig. 46). The output of the electrometer is current-amplified by an emitter follower and is then fed to an inverter, which is normally turned off. When the input is positive, the inverter is turned on, forward-biasing the common emitter amplifier. This in turn forward-biases the base of the output emitter follower and produces a positive output. The electrometer has two linear ranges of 5×10^{-11} and 2.5×10^{-9} amp for a full-scale output deflection. The feedback resistor used to accomplish this range change is selected by a crystal can relay whose power is turned on and off by the mechanical programmer. The dc output from the electrometer amplifier modulates a transformer-coupled 15-v squarewave. The signal on the secondary of the isolation transformer is then demodulated and filtered and fed to the DAS as an analog signal.

The DAS command pulses trigger the lunar programmer one-shot, whose time constant is primarily determined by the 10-μf capacitor. The one-shot holds the

2N1131 transistor switch on, allowing the charged solenoid shunting capacitors to drive the solenoid to the next programmer position. When the 10-μf capacitor has charged to a specific potential, transistors 2N697 and 2N1131 are turned off and remain off until the next trigger pulse from the DAS. Shorting pairs of wipers are advanced across a printed circuit board containing the program by the mechanical programmer. This device is used to apply the bias and retarding potentials to the ion trap and change the electrometer range. A total of 120 indexes constitutes one complete data cycle. Index position 1 delivers a 3-v calibration signal to the DAS so that the start of a data cycle may be identified. Table 4 gives a listing of the range, bias voltage, and retarding potential conditions of the experiment as a function of the programmer index position.

C. *The Power Supply*

The experiment power supply consists of an oscillator which free-runs at 1500 cps when a 28 vdc is applied to the input from the science TR unit and its own TR unit. Most of the transformer secondary voltages are full-wave rectified and filtered for use throughout the electronic package. The 15-v squarewave modulating signal used for data transfer is also derived in this TR unit, as shown in Fig. 46. The output voltage amplitudes from the TR unit are closely regulated by the regulation provided for the 28-vdc input.

Table 4. Programmer index functions

Index No.	Nomenclature	Current range	Spacecraft potential mode, v	Ramp voltage
1	Indexing word (3-v level)			
2-10	Nonretarded 0 mode	Low	0	0 v nonchanging
11-20	Retarded 0 mode	Low	0	Increasing 0 to 30 v
21-30	Retarded −10 mode	Low	−10	Decreasing 30 to 0 v
31-40	Nonretarded −10 mode	Low	−10	0 v nonchanging
41-50	Nonretarded −30 mode	Low	−30	0 v nonchanging
51-60	Retarded −30 mode	Low	−30	Increasing 0 to 30 v
61-70	Retarded −30 mode	High	−30	Decreasing 30 to 0 v
71-80	Nonretarded −30 mode	High	−30	0 v nonchanging
81-90	Nonretarded −10 mode	High	−10	0 v nonchanging
91-100	Retarded −10 mode	High	−10	Increasing 0 to 30 v
101-110	Retarded 0 mode	High	0	Decreasing 30 to 0 v
111-120	Nonretarded 0 mode	High	0	0 v nonchanging

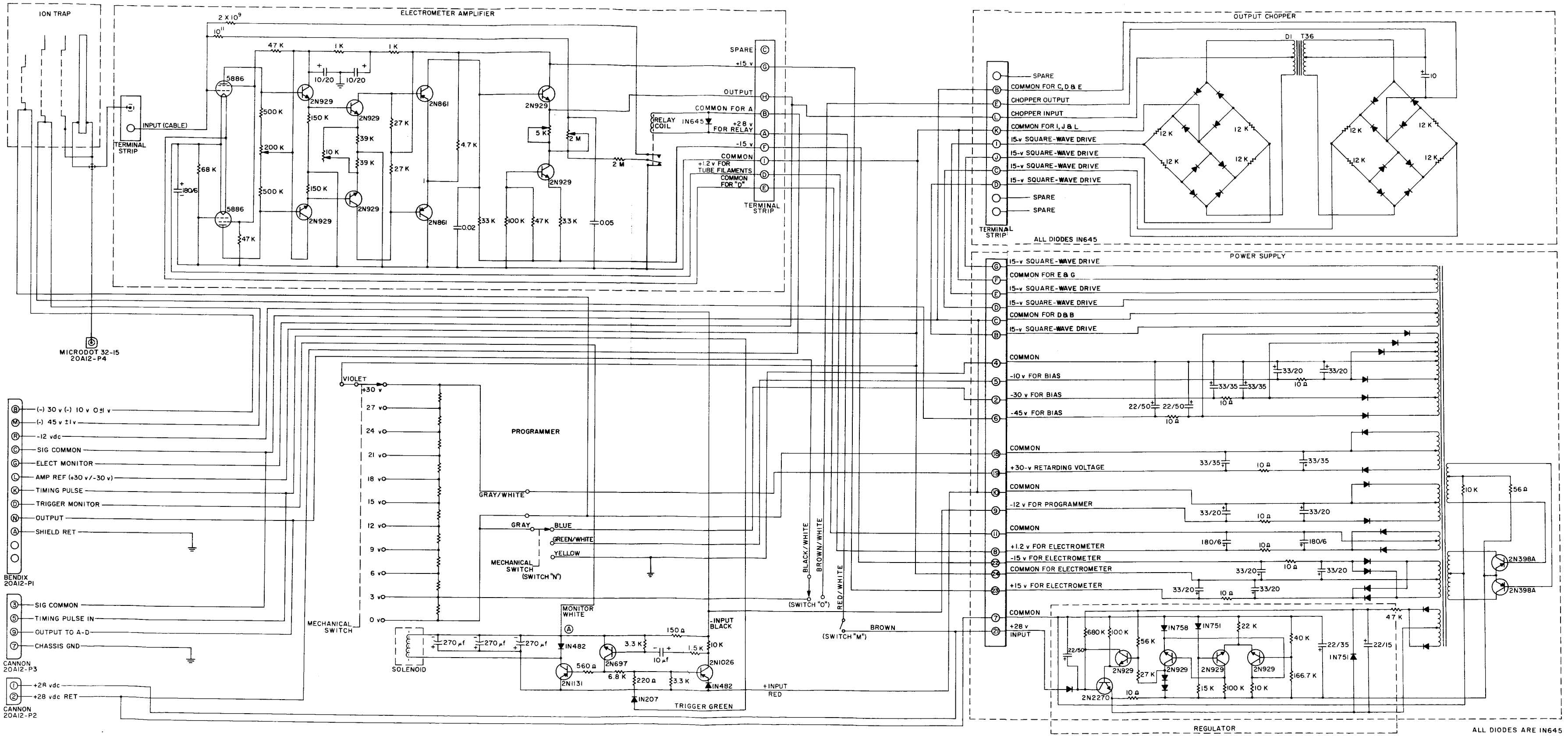


Fig. 46. Low-energy ion detector schematic diagram

XIII. DATA AUTOMATION SYSTEM

The *Ranger* Follow-On data automation system (Fig. 47) is a solid-state electronic system that gathers information from scientific instruments on board the *Ranger* Follow-On spacecraft and prepares it for presentation to telemetry for transmission. Output signals from the scientific instruments are pulse-per-time base, voltage-amplitude, and parallel-binary words. The DAS converts pulse and voltage amplitude data to binary form; suitable timing logic provides for the time-sharing of a single telemetry output channel by all the scientific experiments.

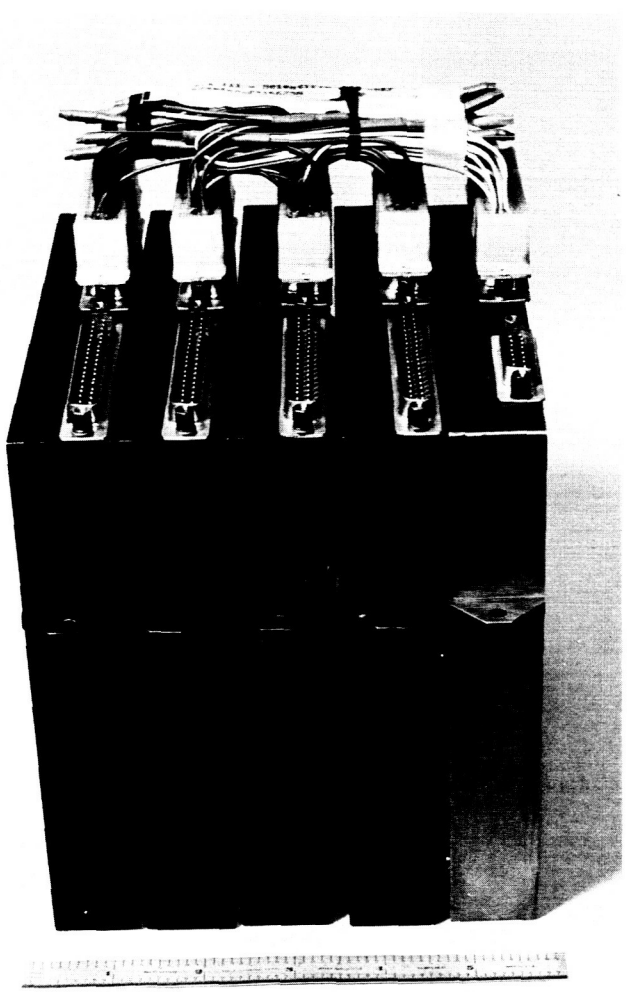


Fig. 47. *Ranger* Follow-On data automation system

The telemetry data are presented as twenty-one 8-bit words. Every two words are presented as an 8-bit data word followed by a 7-bit data word and a parity bit. Each group of 21 words is termed a subframe; a group of 6 subframes is called a master frame; and 8 master frames are called a data cycle. To enable identification of data commutated among subframes, master frames, and data cycles, the output data contain words that number the subframes and master frames. The first two words of each subframe form a pseudonoise sequence to synchronize the data that follow.

A. Physical Description

The DAS consists of 158 modules mounted on five subchassis (or trays): 20A25, 20A24, 20A23, 20A22, and 20A21, each measuring 6.45 by 6 by 1.125 in. Four subchassis are designed to hold 36 modules; the fifth (20A25) is designed to hold 18 modules and the transmit/receive unit. Figure 48 is a top view of subchassis 20A24 (similar to subchassis 20A23 through 20A21), providing module location coordinates. Figure 49 is a top view of subchassis 20A25 which shows module location coordinates in the transmit/receive unit.

B. System Block Diagram

Figure 50 is a block diagram of the DAS. The system derives its basic 25 bits/sec telemetry rate by counting down from the spacecraft 400 cps. Special input circuits modify the 400-cps signal to make it compatible with the DAS circuitry and provide a standby 400-cps source in case of failure of the spacecraft signal. The 400- to 25-cps countdown is performed by flip-flops C1 through C4, whose outputs are decoded to provide timing signals used within the DAS. Flip-flops C5 through C7 form a divide-by-8 counter that forms the basic 8-bit word of the DAS. Flip-flops C8 through C12 form a divide-by-21

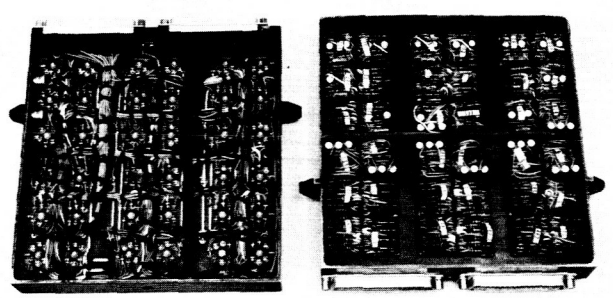


Fig. 48. Subchassis 20A24

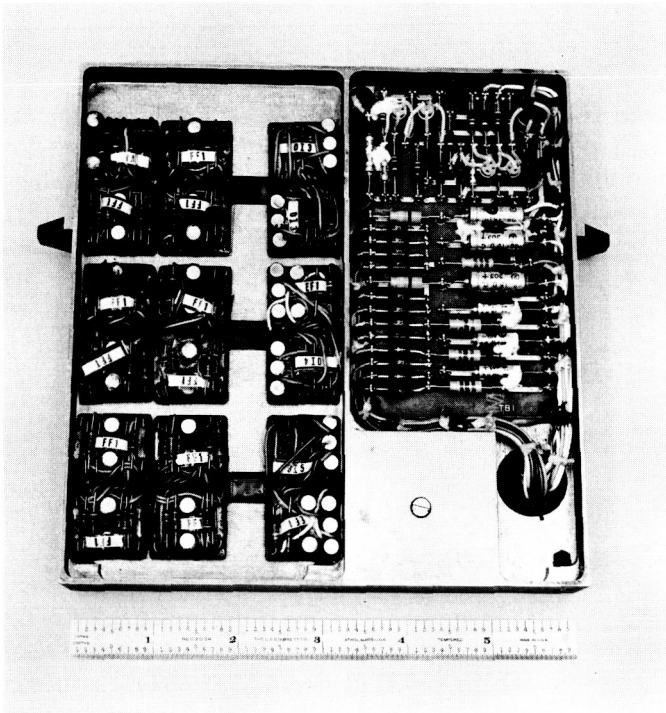


Fig. 49. Subchassis 20A25

counter which, in conjunction with the 5×21 matrix, provides timing pulses for the 21 words that form a subframe. Similarly, C13 through C15 and the 3×6 matrix form the 6 subframes of a master frame, and C16 through C23 form a divide-by-256 counter which counts the master frames. The 2×8 matrix decodes the 8 master frames of a data cycle.

The 8-stage countershift register, SR1 through SR8, is the heart of the data-handling section of the DAS. During words 1 and 2, the outputs of SR7 and SR8 are fed back into SR5 to form the pseudonoise sequence. When used as a counter, flip-flops SR1 through SR8 drive a digital-to-analog converter. The counter outputs are read into the digital-to-analog converter, which develops an analog stairstep voltage. The stairstep voltage is passed to a comparator, where it is compared against a selected analog input. The comparator consists of a crossover detector for each of the analog input channels, with appropriate input gating, and an output amplifier. The output of the comparator disables the counting portion of the countershift register. Thus, the number in SR1 through SR8 is the binary equivalent of the selected input voltage; this number is shifted out to telemetry.

The conversion of the pulse rate inputs to binary form is accomplished with four counters. The three inputs requiring conversions for very low frequencies (COINC, PFI, IC) are counted continuously by two 3-bit counters, KC1 through KC3 and KD1 through KD3, and a 5-bit counter, KB1 through KB5. All intermediate- and high-frequency conversions are performed by time-sharing a single 15-bit counter, KA1 through KA15, which has logic to control the count intervals and select the input to be counted at the proper time. The outputs of all the counters are transferred to SR1 through SR8 at the proper times and shifted out to telemetry. Similarly, the cosmic dust input is transferred in parallel to the shift register and shifted out.

The DAS also generates timing pulses for use by the individual experiments. Certain key signals in the system are provided as outputs to the ground support equipment for checkout purposes.

C. *Experimental Data Handling Techniques*

The scientific instruments on *Ranger* feed three types of data to the DAS: analog, pulses-per-time-base, and parallel binary words. The system samples the analog data and develops the binary equivalent of the input voltage level. Since pulses-per-time-base are counted during specific intervals, the counts represent the pulse rates. The parallel binary words are transferred without conversion.

1. Analog Data Handling

The input analog signal ranges between 0 and +6 v. The output of the analog-to-digital converter is an 8-bit binary number, providing a 23.5-mv resolution of the input voltage level. Analog data readout during odd-numbered words consists of the entire 8 bits. During even-numbered words, the least significant bit of the 8-bit conversion is replaced by the parity bit, producing effectively a 7-bit conversion. The resolution in this case is 47 mv.

For certain of the experiments producing analog outputs, the DAS produces output pulses used as calibration steps and as commutator stepping pulses. Sampling frequencies, conversion accuracies, and pulse outputs for the various analog experiments are detailed in the following paragraphs.

a. Plasma detector. The DAS accepts information from the plasma detector (PD) on five analog channels and performs a 7-bit conversion for each channel. The complete sampling cycle for the plasma detector inputs consists of four complete scans through the group of five

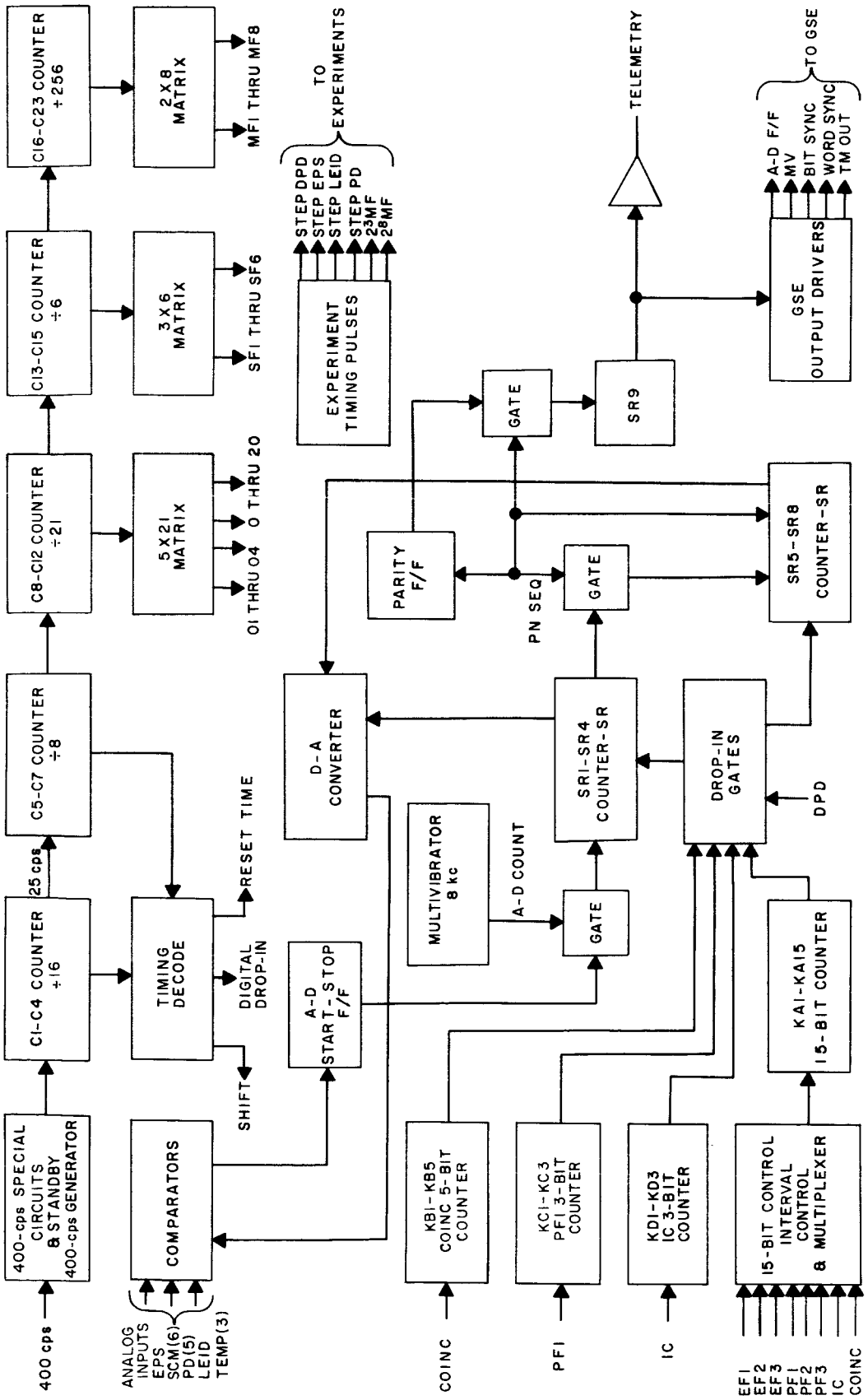


Fig. 50. Data automation system block diagram

inputs. The sampling cycle is repeated once each 40.32 sec. During each scan of the five inputs, the individual channels are converted and read out sequentially at 1.28-sec intervals; i.e., the time from the readout of the most significant bit of the sample from one channel to the corresponding bit of the next channel is 1.28 sec. The time from the start of one scan to the start of the next is 6.72 sec.

A pulse output is provided to step the plasma detector commutator. The stepping pulse occurs at the end of each scan, i.e., after each group of five readouts.

b. Electron-proton spectrometer. The electron-proton spectrometer (EPS) input comes in on a single analog channel and is converted to a 7-bit binary number. During each 40.32-sec interval the DAS provides 10 samplings of the electron-proton spectrometer input voltage level. The 10 samples are split into two groups of 5, the groups separated by a 1.60-sec interval. The samples within each group are spaced at 1.28-sec intervals. A commutator stepping pulse is provided after each sample.

c. Low-energy ion detector. The low-energy ion detector (LEID) input comes in on a single analog channel and is converted to a 7-bit binary number. Twelve readouts are provided per 40.32-sec interval. The readouts are split into three groups of four readouts, the groups separated by 2.88-sec intervals. Samples are spaced within the groups at 1.28-sec intervals. A low-energy ion detector commutator step occurs after each sample.

d. Search coil magnetometer. The DAS samples six analog channels from the search coil magnetometer (SCM) experiment and converts the six voltage levels to 8-bit binary numbers. During each 40.32-sec interval, each channel is sampled and read out once. The channels are sampled sequentially, and the interval between successive samples within a single scan is alternately 2.56 and 4.16 sec. Two calibration pulses are provided for the SCM. One pulse occurs every 2^3 master frames (5.37 min), and the other occurs every 2^8 master frames (172 min), concurrently with the first pulse.

e. Temperatures. The DAS contains provisions for sampling three temperature measurement channels for the following: (1) electron flux, (2) plasma detector, and (3) particle flux. Temperatures are converted to 8-bit binary numbers. Each input is sampled once every 40.32 sec.

f. Spare. A spare analog input is provided and is sampled at three equal intervals during a 20.16-sec period, then is not sampled the next 20.16 sec.

2. Pulse Rate Data Handling

Handling of pulse rate data is accomplished by counting the incoming pulses within specified time intervals. Depending on the frequency range of the pulse inputs and requirements of accuracy and pulse resolution, the inputs are counted over one, two, or three different time intervals. Counting intervals, counter lengths, and readout frequencies for the various experiments are detailed in the following paragraphs.

a. Electron flux. The DAS counts three different electron flux (EF) inputs, each for an interval of 0.92 sec. The 15-bit counter is reset prior to each count, and the total count is sent to telemetry immediately after the completion of the count interval. The three EF counts are performed in a single sequence with readouts spaced at 1.28-sec intervals, i.e., first bit of one readout to first bit of the next. The sequence of three counts is repeated once each 40.32 sec. The 0.92-sec, 15-bit count covers an approximate frequency range of 100 cps to 35 kc.

b. Particle flux 3. The particle flux 3 (PF3) input is covered over the frequency range 0 to 68 kc by counting over three different intervals. The range 0 to 5 cps is covered by performing a continuous 3-bit count, i.e., counting in a 3-bit counter which is never reset. The 3-bit counter is read out on the average of once every 1.34 sec. The readouts are in groups of five with 1.28-sec intervals between readouts; a 1.60-sec interval separates the last readout of a group and the first readout of the next group, yielding the 1.34-sec average. This sequence is repeated continuously.

The 5-cps to 1.6-kc range is covered by performing a 15-bit, 20.16-sec count, starting with a reset counter. This count is performed and read out once each 2.68 min.

The range 1.6 to 68 kc is covered by performing a 0.48-sec count, also in a 15-bit counter which is initially reset. This count is read out once each 40.32 sec.

c. Particle flux 2. The particle flux 2 (PF2) input is covered in the range 5 cps to 68 kc by performing two different counts in a 15-bit counter. The two counts cover the ranges 5 cps to 1.6 kc and 1.6 to 68 kc, respectively; readout is identical to that for PF3 in these ranges.

d. Particle flux 1. The particle flux 1 (PF1) input is handled in a manner identical to that of the PF2 input.

e. Ion chamber. The ion chamber (IC) input is covered in the range 0 to 1.6 kc by performing two different counts. The first count covers the range 0 to 5 cps, and is identical in all respects to the PF3 count for the same range. The range 5 cps to 1.6 kc is covered by a 15-bit count similar to the PF3 count for this range, except that the readout frequency is once per 5.38 min.

f. Coincidence. The coincidence (COINC) input is covered in the range 0 to 68 kc by performing three different counts. The low frequencies (0 to 5 cps) are covered by a continuous 5-bit count. The lower-order two bits of this count are read out at the same frequency as the 3-bit particle flux 3 and ion chamber counts (1.34 sec average). Every 6.72 sec the entire five bits are read out.

The 5-cps to 1.6-kc range is covered by a 20.16-sec, 15-bit count read out every 5.38 min. The 1.6 to 68 kc range is covered by a 0.48-sec, 15-bit count read out every 40.32 sec.

All 15-bit counts are performed in a single 15-bit binary counter using suitable multiplexing and control logic. The low-order stages of the counter are mechanized, using special high-speed flip-flops. This ensures that all high- and intermediate-frequency counts are performed with a double pulse resolution of 4 μsec. Hence, individual input pulses spaced at least 4 μsec apart (leading edge to leading edge) are counted as separate pulses. At the low frequencies, double pulse resolution is not required.

3. Parallel Binary Data Handling

The output of the cosmic dust particle detector is presented to the DAS as a parallel, 6-bit binary number. This number is read out to telemetry once each 40.32 sec. Immediately after each readout, a reset pulse is supplied by the DAS to the experiment.

D. Explanation of Symbols

In the following material, the key letters shown in parentheses refer to Fig. 51.

1. *And* Gates

Two types of *and* gates are used in the DAS: a 4-legged gate (A) and a 3-legged gate (B). Each type has two variations. The bias resistor may take values of 100 K or 22 K. The 4- and 3-legged gates shown in (C) and (D) are connected as 3- and 2-legged *and* gates with an *or* leg output.

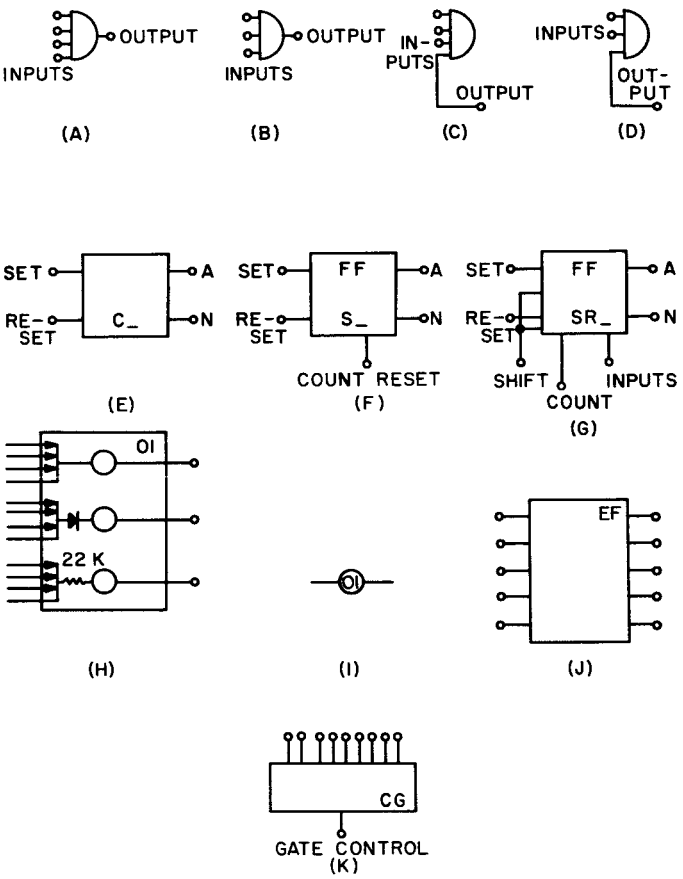


Fig. 51. Data automation system symbols

2. Flip-Flops

Three type of flip-flops are used in the DAS. The symbol for the flip-flop used in the matrix where the only inputs are set and reset is shown in (E). The interval counter flip-flop (F) has an additional input termed the counter reset, which enables resetting of the entire counter. The third type of flip-flop is used in the universal counter and shift register (G). Three sets of inputs are provided: the set-reset input, the shift input, and the count inputs. The count inputs consist of an external CRD gate connected to the bases of the flip-flop transistors.

3. *Or* Inverters

The *or* inverter is shown in (H) and (I). An OI module (H) is comprised of three independent *or* inverter circuits. Three coupling options are provided: direct coupling, diode coupling, and resistor coupling. Each module

may have different combinations of coupling. One module of *or* inverters is shown in (H). A single *or* inverter comprising part of a module is shown in (I). However, owing to logic complexity, the module groups are symbolically ignored.

4. Emitter Followers

Each emitter-follower module contains five emitter followers, as indicated by the symbol (J). Emitter followers are of two types; the types are differentiated by the presence or absence of a 10,000-ohm bias resistor. The use of the resistor is dictated by the characteristics of the circuit driving the emitter follower.

5. CRD Gate

The symbol representing a module of capacitor, resistor, and diode gate circuits used in conjunction with the flip-flop in the universal shift register and counter is shown in (K).

E. Word Descriptions

The DAS performs the basic functions of analog-to-digital conversion, pulse rate conversion, sampling timing, and parallel digital transfer for the scientific instruments on the *Ranger* Follow-On spacecraft. Proper operation of the system provides the following outputs to the ground support and telemetry equipment.

The scientific data are presented as subframes of twenty-one 8-bit words each (see Table 5). Every two words are presented as an 8-bit data word followed by a 7-bit data word and a parity bit. The parity bit provides a means of determining when a data bit is lost during transmission. The first two words of each group of 21 words form a pseudonoise sequence for synchronization of the data that follows.

Each word is described in terms of the 8-bit binary code associated with that output and the octal representation as decoded by the ground support equipment.

Word 1

PN sequence — Word 1 contains the first half of the PN sequence. The binary output is 00001110; the octal output is 016.

Word 2

PN sequence — Word 2 contains the second half of the PN sequence plus the parity bit. The binary output is 11001010; the octal output is 145.

Word 3

Pulse rate conversion — Word 3 contains the results of three different low-frequency pulse rate counts. The first two binary bits and the first octal digit are the lower-order two bits of the COINC 5-bit count. The next three binary bits and the second octal digit are the IC 3-bit count. The last three binary bits and the third octal digit are the PF3 3-bit count. The values of these digits depend on the pulses applied to the COINC, IC, and PF1 inputs.

Word 4

A-D conversion SF1 through SF4 — Word 4 during SF1 through SF4 consists of an A-D conversion for the PD_A input plus parity bit. The output voltage depends on the voltage applied to this input.

SF5 and SF6 — Word 4 during SF5 and SF6 is an A-D conversion for the EPS input plus parity bit. Representative codes for the word 4 A-D conversion are as follows:

Vin	*Binary*	*Octal*
30 mv	0000000P	000
1 v	0010101P	025
3.01 v	0111111P	077
5 v	1101010P	152
6.1 v	0000000P	000

Word 5

A-D conversion SF1 — Word 5 during SF1, is the A-D conversion for the EF temperature.

SF2 — Word 5 during SF2 is the A-D conversion for the PD temperature.

SF3 — Word 5 during SF3 is the A-D conversion for the PF temperature. Representative codes are as follows:

Vin	*Binary*	*Octal*
30 mv	00000001	001
1 v	00101011	053
3 v	01111111	177
5 v	11010101	325
6.1 v	00000000	000

Pulse rate conversion SF4 through SF6 — Word 5 during SF4 through SF6 corresponds to the eight most significant bits of 15-bit counts which are commutated as follows:

SF4 — MF1-MF5 and PF1, 20.16-sec count. MF2 and MF6-PF2, 20.16-sec count. MF3 and MF7-PF3, 20.16-sec count. MF4 COINC, 20.16-sec count. MF8-IC, 20.16-sec count.

SF5 — COINC, 0.48-sec count.

SF6 — EF1, 0.92-sec count.

Word 6

A-D conversion SF1 through SF3 — Word 6 during SF1 through SF3 is the A-D conversion for the LE1D input plus the parity bit. Representative codes are as in the word 4 A-D conversion.

Pulse rate conversion SF4 through SF6 — Word 6 during SF4 through SF6 corresponds to the seven least significant bits of 15-bit counts which are commutated as in word 5, SF4 through SF6.

Word 7

Pulse rate conversion — Same as word 3.

Word 8

A-D conversion — Same as word 4 except PD input is PD_B.

Word 9

A-D conversion SF1 through SF3 — Word 9 during SF1, SF2, and SF3 is the A-D conversion for SCM1, SCM3, and SCM5, respectively. Representative codes are as in word 5.

Parallel digital transfer SF4 — The first two bits of word 9 during SF4 are blank. The remaining six bits and the corresponding two octal digits are the CDD 6-bit parallel readout.

SF 5 — Word 9 during SF5 is blank.

Pulse rate conversion SF6 — Word 9 during SF6 is the eight most significant bits of the EF2 15-bit, 0.92-sec count.

Word 10

A-D conversion SF1 through SF3 — Same as word 6.

SF4 and SF5 — Blank.

Pulse rate conversion SF6	Word 10 during SF6 is the seven least significant bits of the EF2 15-bit, 0.92-sec count plus parity bit.
Word 11	Same as word 3.
Word 12	Same as word 4 except PD input is PD_C.
Word 13	
A-D conversion SF1 through SF3	Word 13 during SF1, SF2, and SF3 is the A-D conversion for the analog spare input.
Parallel data transfer SF4	During SF4, word 13 is the main frame count. Its value increases by one each readout.
SF5	Blank.
SF6	Word 13 during SF6 is the eight most significant bits of the EF3 15-bit, 0.92-sec count.
Word 14	
A-D conversion SF1 through SF3	Same as word 6.
SF4 and SF5	Blank.
Pulse rate conversion SF6	Word 14 during SF6 is the seven least significant bits of the EF3 15-bit, 0.92-sec count plus parity bit.
Word 15	
Pulse rate conversion	Same as word 3.
Word 16	
A-D conversion	Same as word 4 except PD input is PD_D.
Word 17	
A-D conversion SF1 through SF3	Word 17 for SF1, SF2, and SF3 is the A-D conversion for SCM2, SCM4, and SCM6, respectively. Representative codes are as in word 5.
Pulse rate conversion SF4 through SF6	During SF4 through SF6, word 17 is eight most significant bits of a commutated 15-bit, 0.48-sec count. Commutation is as follows: SF4-PF1, SF5-PF2, and SF6-PF3.
Word 18	
A-D conversion SF1 through SF3	Same as word 6.
Pulse rate conversion SF4 through SF6	During SF4 through SF6 word 18 is the seven least significant bits of a commutated 15-bit count plus the parity bit. Commutation is as in word 17 above.
Word 19	
Pulse rate conversion	Same as word 3.
Word 20	
A-D conversion	Same as word 4 except PD input is PD_S.
Word 21	
Pulse rate conversion	The first five bits and the first two octal digits of word 21 are 5-bit COINC count. The remaining three bits and octal digit are the SF count. This readout increases by one each time until it reaches 5, at which time it returns to zero.

Table 5. Ranger Follow-On data automation system, master frame format

WORD	1 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
SF 1	(PN)	C IC PFD 3	PD	Temp 1	LEID	C IC PFD 3	PD	SCM 1	LEID	C IC PFD 3	PD	——	LEID	C IC PFD 3	PD	SCM 2	LEID	C IC PFD 3	PD	C SFC
SF 2	↓	↓	PD	Temp 2	LEID	↓	PD	SCM 3	LEID	↓	PD	——	LEID	↓	PD	SCM 4	LEID	↓	PD	↓
SF 3			PD	Temp 3	LEID		PD	SCM 5	LEID		PD	——	LEID		PD	SCM 6	LEID		PD	
SF 4			PD	Commutated			PD	—CDD	——		PD	MFC	——		PD	(PFD 1 HF)			PD	
SF 5			EPS	(C HF)			EPS	——	——		EPS	——	——		EPS	(PFD 2 HF)			EPS	
SF 6	↓	↓	EPS	(EFD 1)		↓	EPS	(EFD 2)		↓	EPS	(EFD 3)		↓	EPS	(PFD 3 HF)		↓	EPS	↓

Abbreviations:

C	Coincidence (PFD 2 and 3)
CDD	Cosmic dust detector
EFD	Electron flux detector
EPS	Electron-proton spectrometer
HF	High frequency (0.48 sec on 15-bit counter)
IC	Ion chamber
IF	Intermediate frequency (20.16 sec on 15-bit counter)
LEID	Low-energy ion detector
MF	Master frame
MFC	Master frame count (0 to 255)
PFD	Particle flux detector
PN	Pseudonoise (000011101100101)
SCM	Search coil magnetometer
SF	Subframe
SFC	Subframe count (0 to 5)
PD	Plasma detector

Temp 1—EFD
Temp 2—PD
Temp 3—PFD

Commutated words 5 and 6 (SF 4):

MF 1	PFD 1 1F
MF 2	PFD 2 1F
MF 3	PFD 3 1F
MF 4	C 1F
MF 5	PFD 1 1F
MF 6	PFD 2 1F
MF 7	PFD 3 1F
MF 8	IC 1F

1 Master frame = 6 subframes = 126 words = 1008 bits = 40.32 sec
1 Master frame = 6 SF 1 SF = 21 W 1 W = 8 B 1 B = 40 millisec
= 40.32 sec = 6.72 sec = 0.32 sec

Odd-numbered words = 8 bits
Even-numbered words = 7 bits + 1 parity (odd) bit

( ) Indicates 2-word readout
\+ Indicates repetition
— Represents zero readouts

F. Subchassis 20A21

Subchassis 20A21 contains the analog-to-digital converter (see the logic diagram in Fig. 52). The reference supply for the converter generates a precision 6 v that is switched by the eight stages of the digital-to-analog converter. The digital-to-analog converter is actuated by the outputs of shift register flip-flops SR1 through SR8, which are buffered through emitter followers. The converter output is a thevenized voltage whose value depends on the code in the shift register. The output of the digital-to-analog converter is fed into the 18 comparators, whose outputs are tied in common. Each comparator input is tied to an analog signal and three input select lines. When all three logic lines are true, the analog input is compared with the digital-to-analog converter output.

To perform an analog-to-digital conversion, the proper input select lines are actuated, and the analog-to-digital flip-flop (subchassis 20A24) is set, permitting the shift register to count. As the shift register counts the 8-kc pulses produced by a multivibrator, the output voltage from the digital-to-analog converter becomes progressively more positive. When the voltage passes the selected analog input, an output change occurs and is amplified by the complementary amplifier and the comparator output, and a pulse which resets the analog-to-digital converter is produced. The number left in SR1 through SR8 is then the digital equivalent of the analog input. This number is shifted out to telemetry.

To prevent a spurious comparison (which might occur during carry propagation in the countershift register), the comparators are strobed at the trailing edge of the multivibrator output. (The count occurs at the leading edge of the multivibrator output.) Both the strobe and the count are gated by the analog-to-digital flip-flop; thus the comparison and count may occur only during a selected analog-to-digital conversion time.

Additional logic for resetting the analog-to-digital converter is provided by an *or* inverter. The $\overline{SR8}$ line into the OI provides for resetting the analog-to-digital converter when SR8 goes through a set-to-reset transition and thus provides the means for stopping the conversion when the counter overflows. Reset occurs at the end of the first bit of each word, except during a pseudonoise sequence. Reset ensures that a malfunction of the digital-to-analog count (resulting in the failure of the digital-to-analog voltage to exceed the analog input) will not otherwise affect the operation of the system.

G. Subchassis 20A22

Subchassis 20A22 contains the counters used to perform the pulse-rate-to-digital conversions and the control logic associated with these counters (see the logic diagram in Fig. 53).

The 15-bit counter is time-shared among all inputs requiring conversion in the high- and intermediate-frequency ranges. Each pulse input is gated with appropriate timing logic in one or two *and* gates, depending on whether one or two different count intervals are required for the particular input. The outputs of all *and* gates are buffered by two *or* inverters, together with the *or* logic provided by the input gates of KA1.

Signals MF1, MF2, MF3, and MF4 (generated in subchassis 20A25) are each true for the first three subframes of two different master frames, as follows:

MF1: master frames 1 and 5, subframes 1 through 3

MF2: master frames 2 and 6, subframes 1 through 3

MF3: master frames 3 and 7, subframes 1 through 3

MF4: master frames 4 and 8, subframes 1 through 3

The subframe 1 through 3 interval is the basic 20.16-sec interval required for the intermediate frequency counts. Thus PF1, PF2, and PF3, gated with MF1, MF2, and MF3, respectively, provide for the two intermediate frequency counts per data cycle on each of these inputs. Coincidence is gated with MF4 and $\overline{C18}$ to enable the count during master frame 4 only. IC is gated with MF4 and C18 to enable the count during master frame 8 only.

The signal 48S (from subchassis 20A24) defines the basic 0.48-sec counting interval required for the high-frequency conversions on the particle flux, coincidence, and ion chamber inputs. This signal is true, starting halfway through every 03 time and extending through the following 04 time, for a total duration of 12 bit times. Coincidence is gated with this signal and with the logic signal *zero* to perform the high-frequency count during words 3 (second half only) and 4, for drop-in into the shift register during words 5 and 6. The inclusion of the term SF5 ensures that this count will occur during subframe 5 only, as required by the data format. In a similar fashion, PF1, PF2, and PF3 are gated with "12" and SF4, SF5, or SF6, to perform the 0.48-sec count during words 15 and 16 for the appropriate subframes.

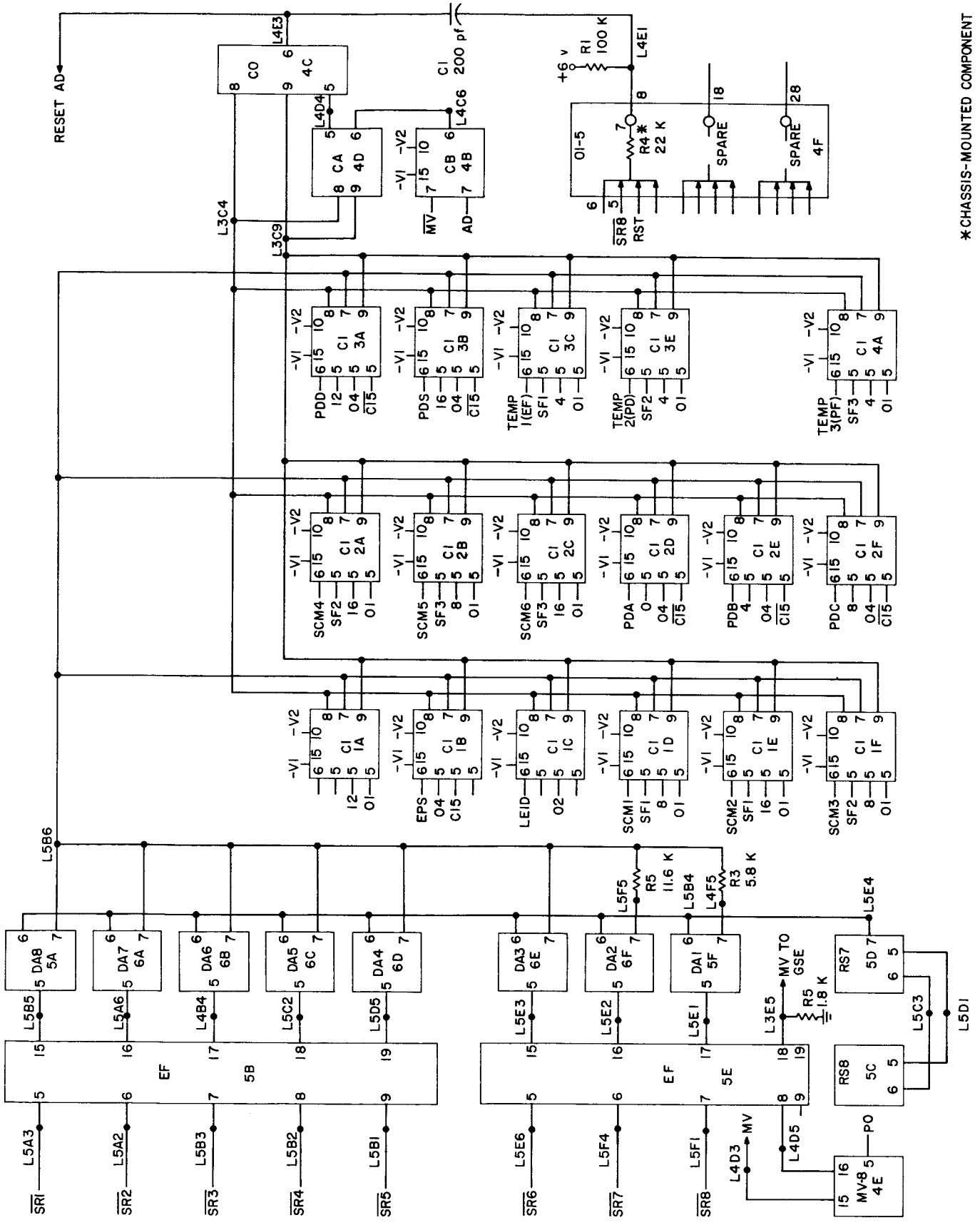


Fig. 52. Subchassis 20A21 logic diagram

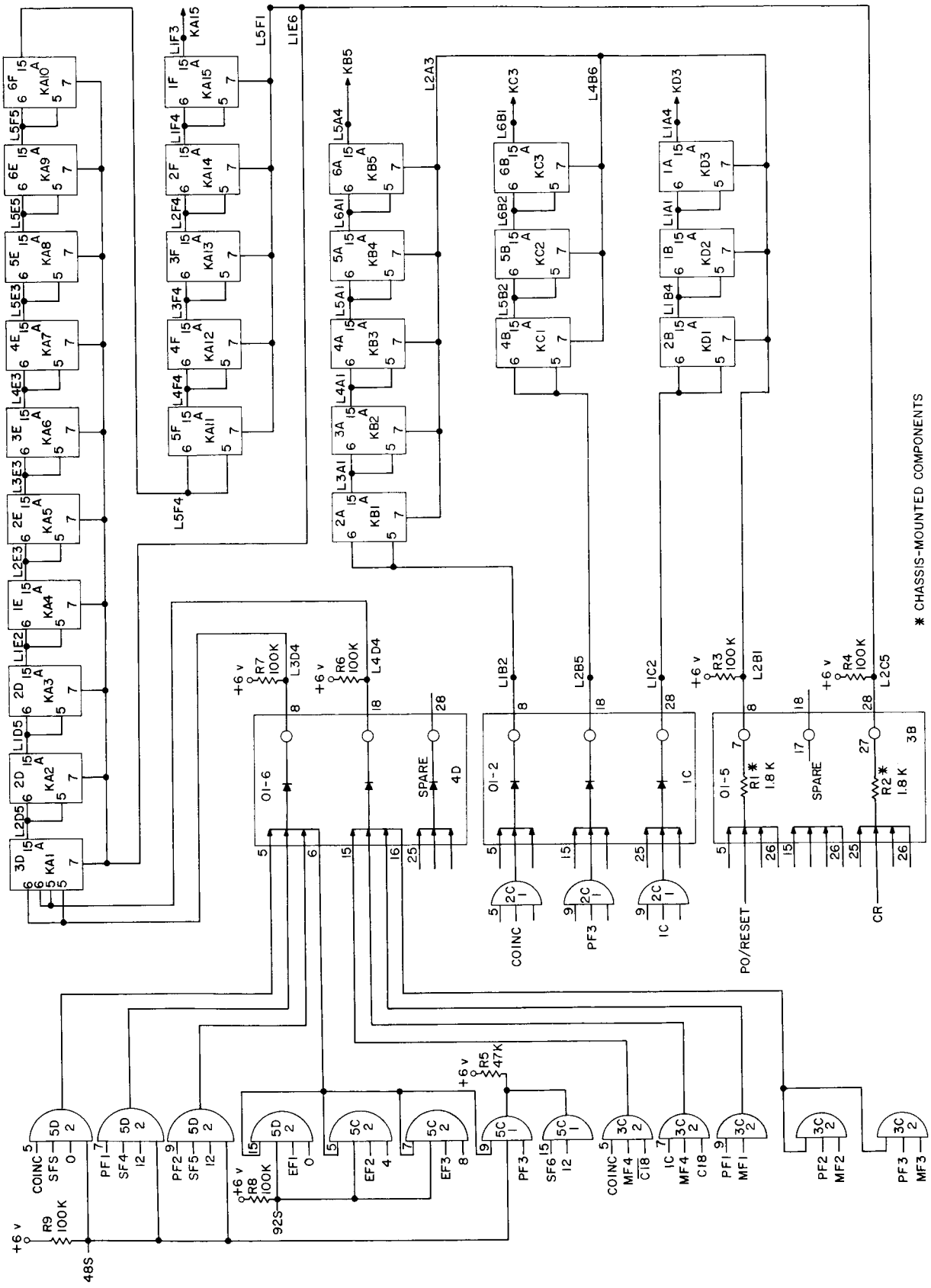


Fig. 53. Subchassis 20A22 logic diagram

The 0.92-sec EF counts are enabled in a similar fashion. The signal 92S, also generated in subchassis 20A24, is true for periods starting with the second bit of 02 and extending through 03 and 04, but only during subframe 6. The pulse inputs EF1, EF2, and EF3 are gated with 0, 4, or 8 to enable the count during the appropriate groups of words.

The reset signal (CR), for the 15-bit counter is generated in subchassis 24. Its timing is discussed in the following section. The counter reset is buffered through an *or* inverter in 20A22, and is applied to the reset lines of the 15-bit counter. Counters KB (5 bits), KC (3 bits), and KD (3 bits) perform the continuous low-frequency counts for the coincidence, PF1, and ion chamber inputs, respectively. Each of the three inputs is brought in, through an *and* gate and an *or* inverter, for noise protection. These three counters are reset by the power on (PO) reset only, which is buffered through an *or* inverter.

H. Subchassis 20A23

Subchassis 20A23 contains the countershift register, the digital dump circuits, the pseudonoise sequence circuits, and the parity and analog-to-digital flip-flops (see the logic diagrams in Fig. 54 ab).

Flip-flops SR1 through SR8, together with their associated CG gates, form the countershift register. The outputs are shifted from left to right (from SR1 through SR8) when shift pulses are applied, unless an analog-to-digital conversion is in process (analog-to-digital flip-flop set). During a conversion, the shift is disabled and the multivibrator count pulses (from subchassis 20A21) are gated with AD and applied to SR1 as the count input.

When a pseudonoise sequence is generated, the outputs of SR7 and SR8 are fed back to the input of SR5. A *one* is read into SR5, provided the outputs of SR7 and SR8 are identical; otherwise, a *zero* is read into SR5. The circuits for determining when a pseudonoise sequence is to be generated are located on subchassis 20A24.

Normally, the output of SR8 is shifted into SR9 (the buffer between the shift register and the telemetry output circuit) and simultaneously into PFF, as a complement input. During PT (from a subchassis 20A24), the output of PFF is shifted into SR9 as the parity bit. The output of PFF is also used at this time as its own complement input, providing for the reset at the end of each even-numbered word.

The parallel drop-in of data into the shift register is accomplished by grounding the negation outputs of the flip-flops which will store a *one*. The outputs of an *or* inverter are tied to each stage ($\overline{SR1}$ through $\overline{SR8}$). If at the time the digital dump pulse (DD) occurs, one of the input legs of a given *or* inverter is *one*, the inverter output will go to ground, setting the corresponding flip-flop.

The input legs of the *or* inverters are conditioned by a set of *and* gates. For each *or* inverter there is a gate corresponding to each data word which drops into the particular shift-register stage. To drop a word into the register at a given time (as defined by the data format), the gates corresponding to all the bits in that word are enabled simultaneously by the various matrix lines gated with the data. Register loading precedes the digital dump pulse. Note that the drop-in logic for the 15-bit counter shows the contents of the counter being dropped into the shift-register during every 01 and 02 times of subframes 4, 5, and 6, although the data format shows that some of these times are blank and that the DPD and MFC readouts should occur during others. At the times when a high- or intermediate-frequency count is to be read out, the 15-bit counter contains the count, but all other times the counter contains all *zeros*. Thus, the blank readouts will be all *zeros*, and the superposition of the readout of the KA counter upon the DPD and MFC readouts will have no effect upon the latter.

The set logic for the analog-to-digital flip-flop is similar to that of the digital drop-in logic. Logic at the input of an *or* inverter defines the words during which analog-to-digital conversions are to be performed, and the occurrence of digital dump when the words are present sets the analog-to-digital flip-flop, initiating the conversion. The reset logic for AD is described in the discussion of subchassis 20A21.

I. Subchassis 20A24

Subchassis 20A24 contains the first 12 stages of the data sync counter, the 21-word matrix, the experiment step output drive circuits, the 400-cps input circuits, and a number of circuits for generating various timing signals used within the DAS (see the logic diagrams in Fig. 55 ab).

The 400-cps circuits include noise protection circuits and a free-running multivibrator which is normally triggered by the 400-cps input. In the event of failure of this input, the multivibrator provides for a standby clock. Free running, it has a frequency of approximately 394 cps.

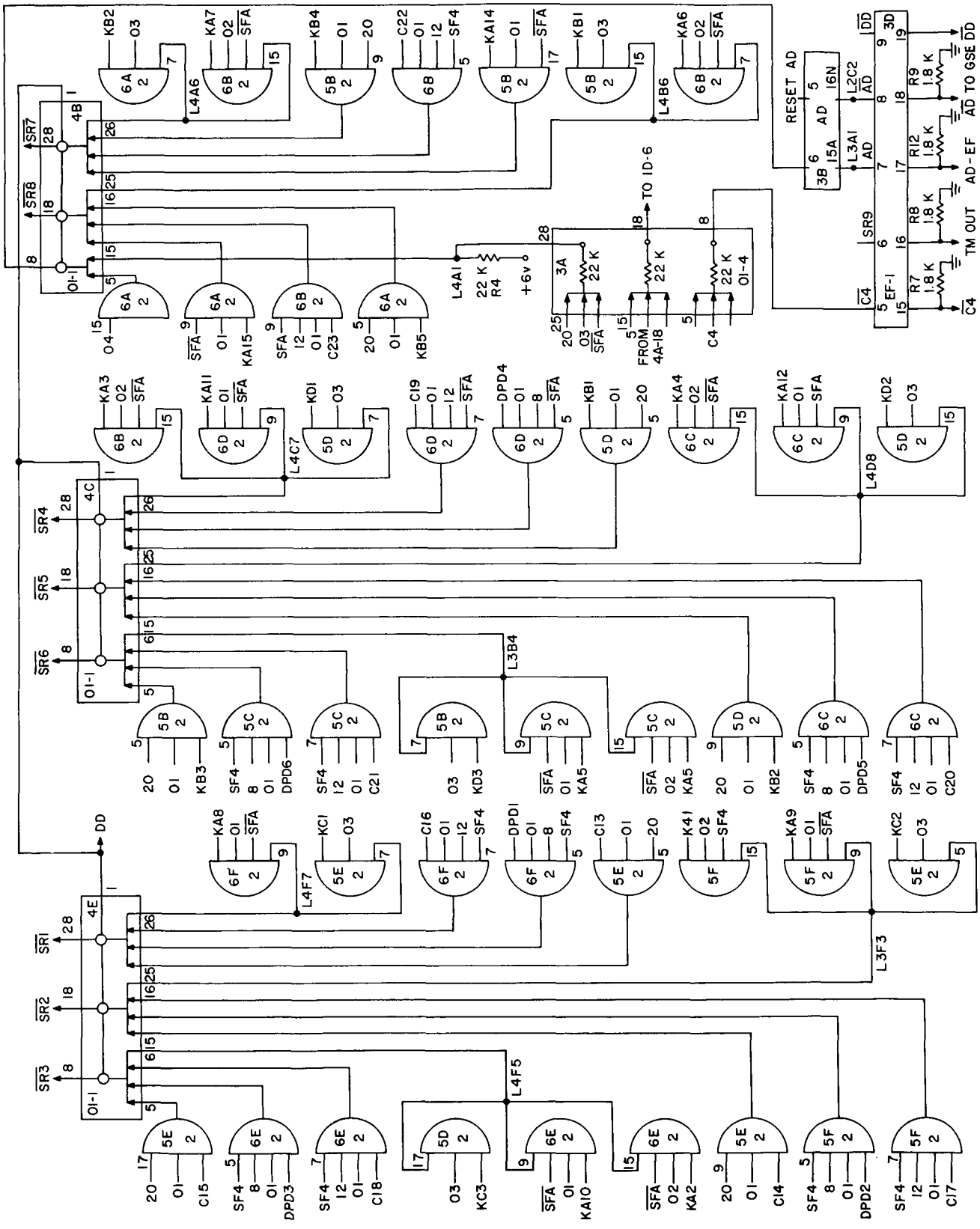
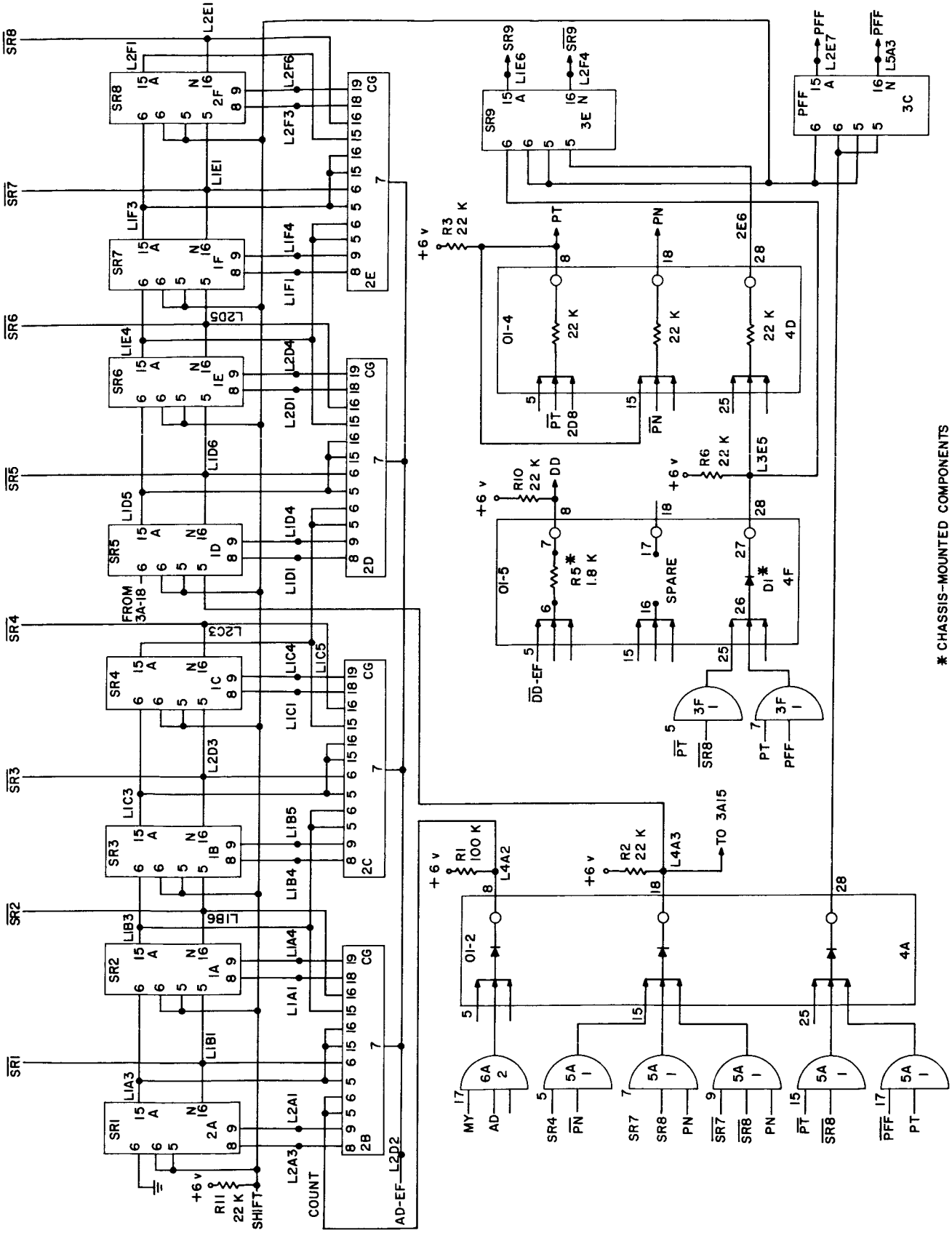


Fig. 54a. Subchassis 20A23 logic diagram



* CHASSIS-MOUNTED COMPONENTS

Fig. 54b. Subchassis 20A23 logic diagram

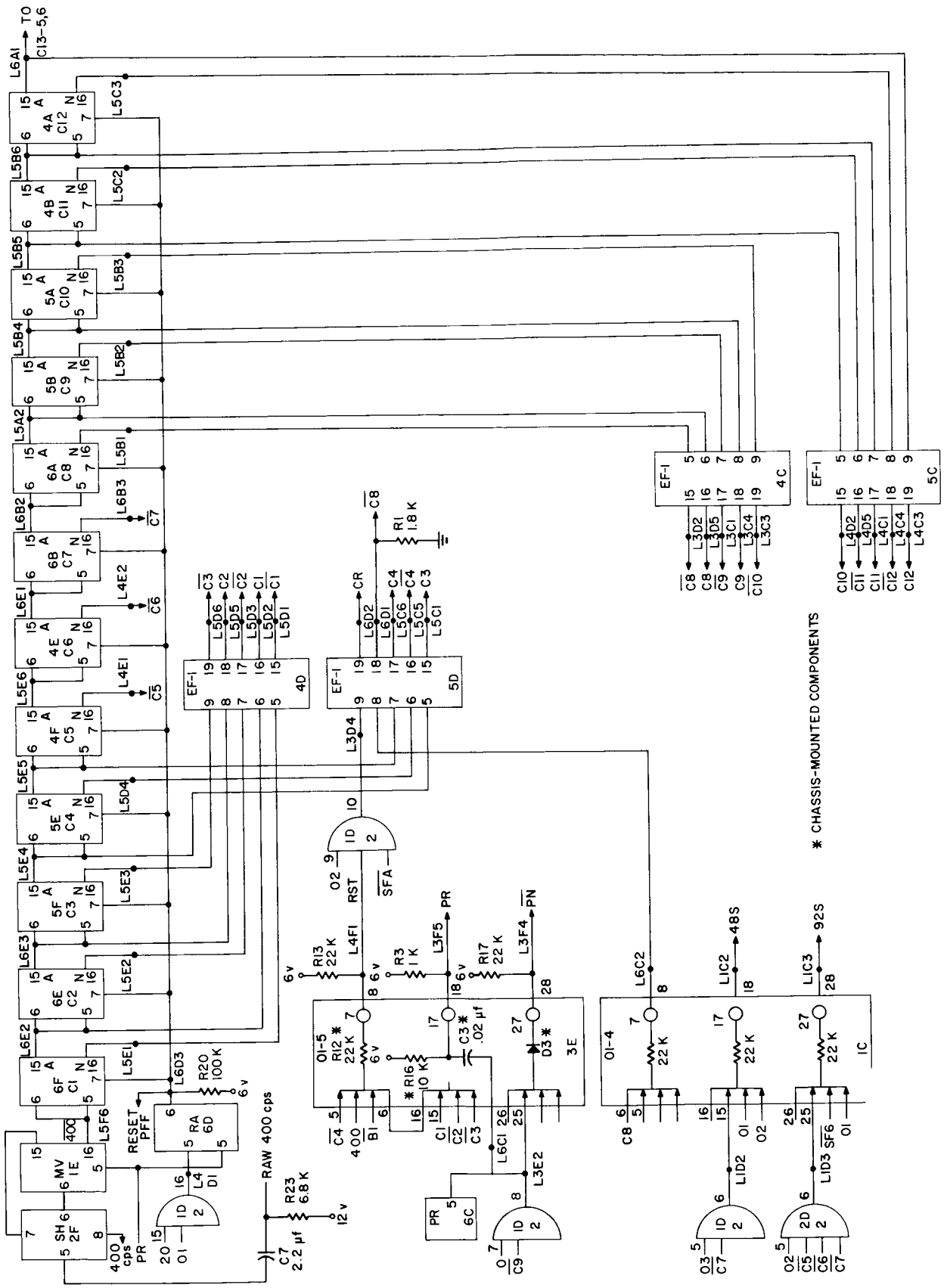


Fig. 55a. Subchassis 20A24 logic diagram

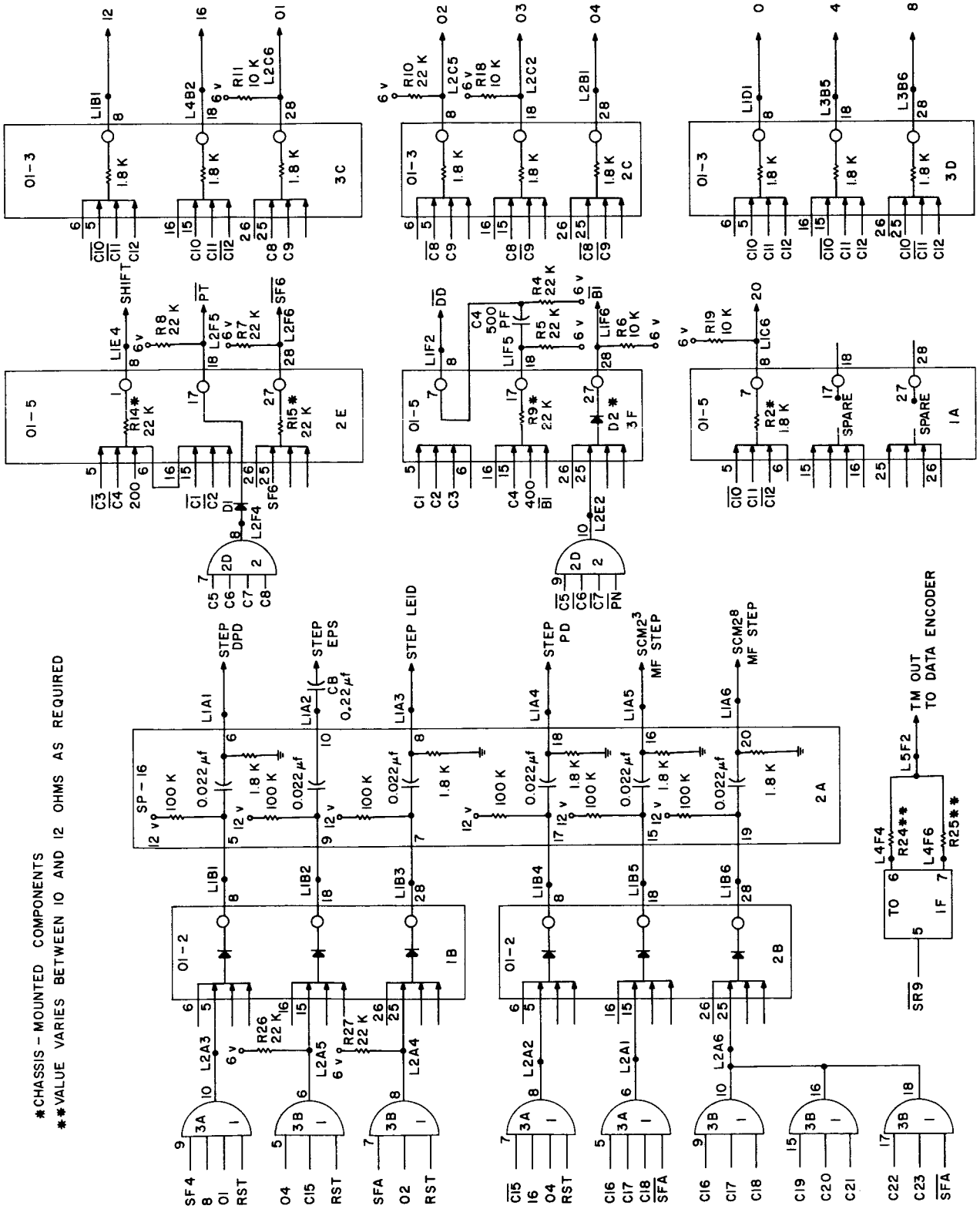


Fig. 55b. Subchassis 20A24 logic diagram

Flip-flops C1 through C4 form a divide-by-16 counter which counts down the 400-cps clock rate to provide the basic 25-cps bit rate. The 25-cps signal is the input to C5 through C7, which is a divide-by-8 counter defining the 8 bits of each word. This in turn drives C8 through C12, the divide-by-21 counter forming the 21 science words for each subframe. The reset amplifier in module 6D resets C1 through C12 at the end of word 21. The outputs of these counter stages are buffered through emitter followers for use in the decoding matrices and timing logic.

The outputs of the divide-by-21 counter drive *or* inverters which form the 5-by-21 matrix. The matrix is divided into two sections. Flip-flops C8 and C9 drive a 2-by-4 matrix which produces outputs 01, 02, 03, and 04. Flip-flops C10, C11, and C12 drive a 3-by-6 matrix, which produces outputs 0, 4, 8, 12, 16, and 20. The words are derived from the *and*ing of the outputs of both matrices as follows:

Word 1	0 and 01	Word 12	8 and 04
Word 2	0 and 02	Word 13	12 and 01
Word 3	0 and 03	Word 14	12 and 02
Word 4	0 and 04	Word 15	12 and 03
Word 5	4 and 01	Word 16	12 and 04
Word 6	4 and 02	Word 17	16 and 01
Word 7	4 and 03	Word 18	16 and 02
Word 8	4 and 04	Word 19	16 and 03
Word 9	8 and 01	Word 20	16 and 04
Word 10	8 and 02	Word 21	20 and 01
Word 11	8 and 03		

Various timing signals are generated in the *or* inverter modules together with their associated *and* gates. $\overline{B1}$ is false during only the first bit of all words (except words 1 and 2), and is used in the generation of DD and RST. The digital dump signal, DD, occurs during the first of the sixteen 400-cps pulses, which are counted to form a 25-cps pulse for the first bit of every word except the pseudonoise words (1 and 2).

The digital dump pulse is generated by a one-shot to provide a narrow drop-in pulse. Reset occurs during the 15th of these same sixteen pulses, and SHIFT occurs during the sixteenth. Thus, the 25-cps clock may be thought of as a sixteen-phase clock, with DD, RST, and SHIFT being the 1st, 15th, and 16th phases, respectively, all gated with B1. Note that the right shift of the counter-shift register occurs on the trailing edge of the *shift* signal, which is simultaneous with the advancement of the data sync counter.

Reset is gated with 02 and $\overline{SFA}$, then buffered through an emitter follower to form counter reset, the reset signal for the KA counter. Counter reset occurs at the end of the first bit of words 6, 10, 14, and 18 during subframes 4, 5, and 6.

Parity timing and pseudonoise define the times at which the parity bit and the pseudonoise sequence are to be read out. Parity timing is true for the 8th bit of every even-numbered word, and pseudonoise is true for words 1 and 2. The negations of these signals are formed on this subchassis (20A24).

The experiment step outputs are generated by differentiating the outputs of *or* inverters, which are driven by appropriate timing signals. The differentiating network for all step outputs are located in a single module. Step DPD occurs during reset for word 9 during subframe 4, i.e., immediately after each digital dump for the cosmic dust particle detector readout. Similarly, steps EPS and LEID occur after all analog-to-digital conversions for these inputs. Step PD occurs after every 5th PD conversion (word 20). The 2^3 and 2^8 MF steps occur at the end of subframe 3 for every 8th and 256th master frame, respectively.

J. Subchassis 20A25

Subchassis 20A25 contains the subframe and master frame counters and the associated matrix logic (see the logic diagram in Fig. 56).

C13 through C15 is a divide-by-six counter that enables the six subframes of each master frame. The word counter on subchassis 20A24 drives C13 through C15, which in turn drives the 8-bit master frame counter C16 through C23. The outputs of these counter stages are buffered through emitter followers for decoding. A reset amplifier driven from the power-on reset module (subchassis 20A24) provides for the reset of C13 through C23.

The *or* inverters are the 3-by-6 matrix which forms the subframe lines SF1 through $\overline{SF6}$, each of which is true for an entire subframe. These subframe lines are combined to form SFA and $\overline{SFA}$, which are true for the first three and last three subframes of each master frame,

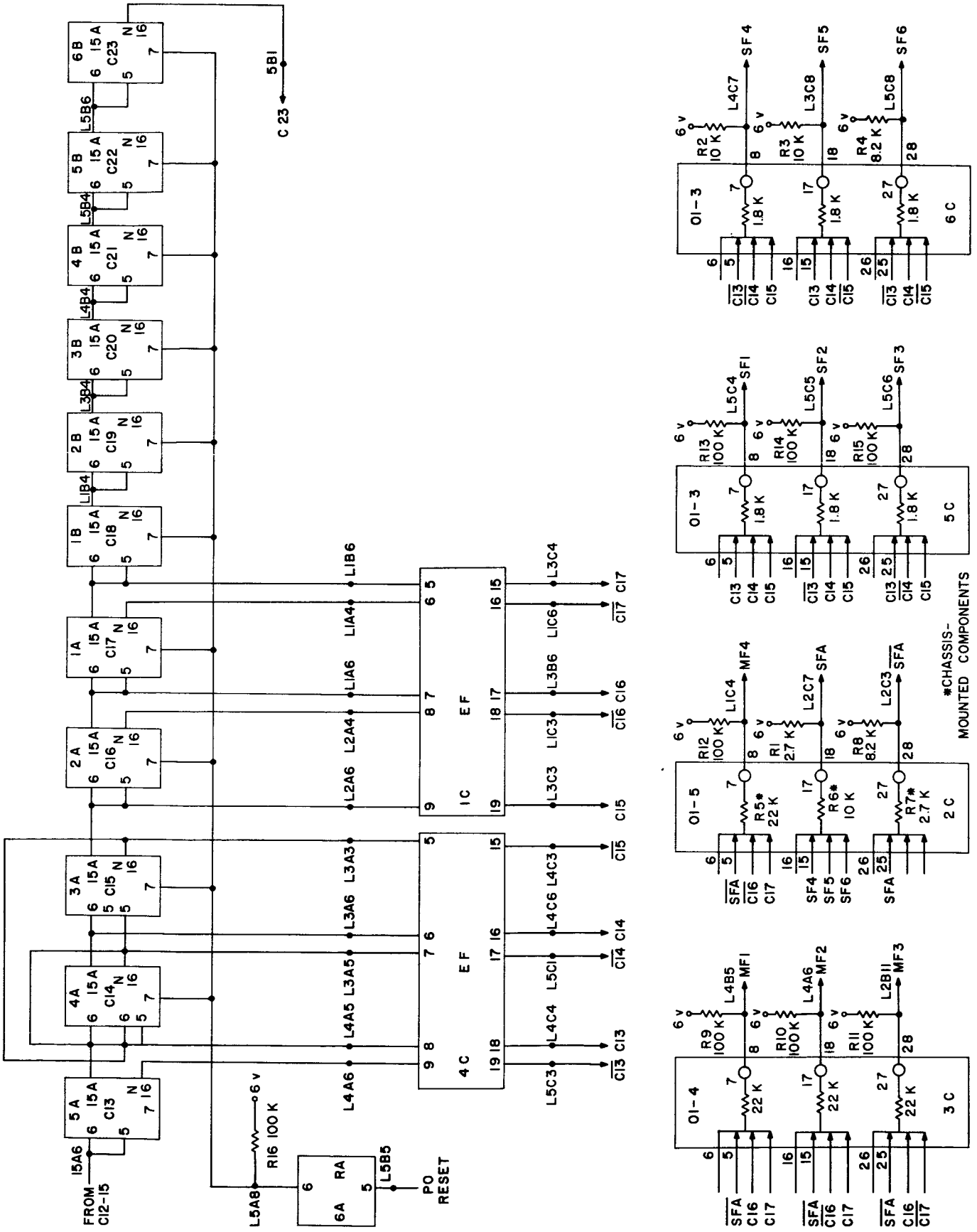


Fig. 56. Subchassis 20A25 logic diagram

respectively. The signals MF1 through MF4 provide the requisite master frame decoding.

K. Circuit Descriptions

1. Flip-Flop

Figure 57 is the schematic diagram of the basic flip-flop used in the DAS. When transistor Q1 conducts, the collector is at 0.3 v. Resistors R4 and R6 comprise a divider network, biasing transistor Q2 off. When Q2 is off, Q1 is biased on, owing to the current through resistors R1 and R3. When Q2 conducts, the collector is at 0.3 v. When Q1 is biased off, Q2 is biased on by the current through resistors R2 and R4. To change the state of the flip-flop, the input to the conducting transistor must be pulled from 3 v to ground.

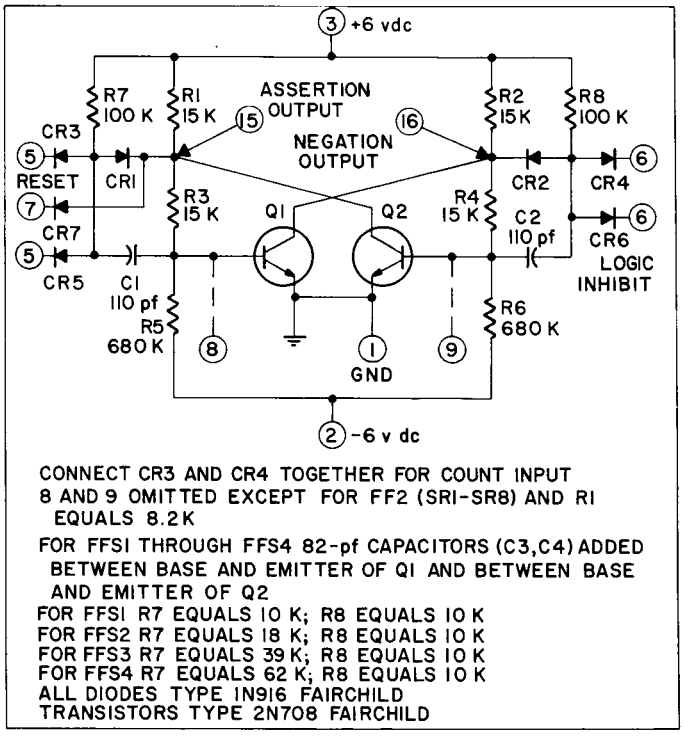


Fig. 57. Flip-flop schematic diagram

To form a count, connect lead 5 to lead 6. When Q2 conducts, the collector is at 0.3 v and the plate of diode CR1 is at 0.9 v. The collector of Q1 is at 3 v, the potential fixed by divider of R2 and R4, and the plate of diode CR2 is at 3.6 v. When the input goes from 3 v to ground, the plate of diode CR2 is pulled from 3.6 v to ground, turning transistor Q2 off and Q1 on. During the next pulse, the plate of diode CR2 is at 0.9 v and the plate of CR1 is at 3.6 v. The second pulse turns Q1 off and turns Q2 on, resulting in a basic divide-by-2 counter.

Leads 8 and 9 are connected to the capacitor diode gate for countershift register SR1 through SR8. For the first four stages of the input digital counter, flip-flops S1 through S4, the circuit is slightly modified to allow operation at a faster speed.

2. Capacitor Diode Gate

The capacitor diode gate (Fig. 58) is used as an alternate method of gating into flip-flops. If leads 8 and 9 are connected to leads 8 and 9 of the flip-flop, the gate can change the state of the flip-flop. For countershift register operation, the shift pulses are applied to leads 5 and 6 of the flip-flop. These pulses are gated off to inhibit the shifting of the register. When the gate control input, lead 7, is returned to 3 v, the capacitor diode gate acts as a count input to SR1 through SR8. The cathodes of CR2 and CR3 are tied to a 2.4-kc pulse source. Diode CR1 is connected to the flip-flop assertion output and CR4 is connected to the flip-flop negation output. The gate control input is tied to an emitter follower. When the emitter follower output is at 3 v, capacitors C1 and C2 can charge and discharge, and the flip-flop counts because of the energy transition applied through the capacitor diode gate. When the count input is to be inhibited, the gate control input is grounded. The capacitor cannot be charged; therefore, no changes can occur in the flip-flop owing to the capacitor diode gate.

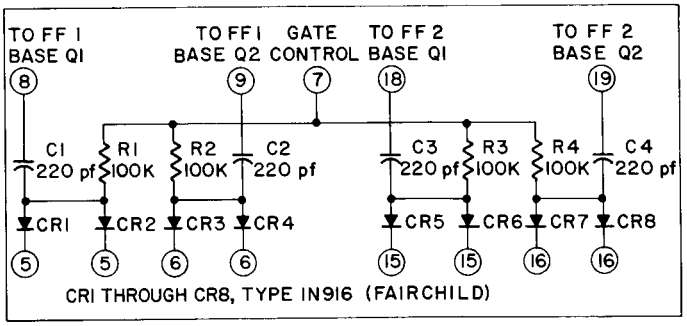


Fig. 58. Capacitor diode gate schematic diagram

3. *And* Gate 4

The *and* gate (Fig. 59) is comprised of four *and* circuits, each of which has four inputs and one output. Resistors R1 through R4 are 22 or 100 kilohms, depending on the output load. Where the *and* gate is driving an *or* gate that does not have an input diode available, the

output is taken off of one of the *and* gate input diodes (lead 5).

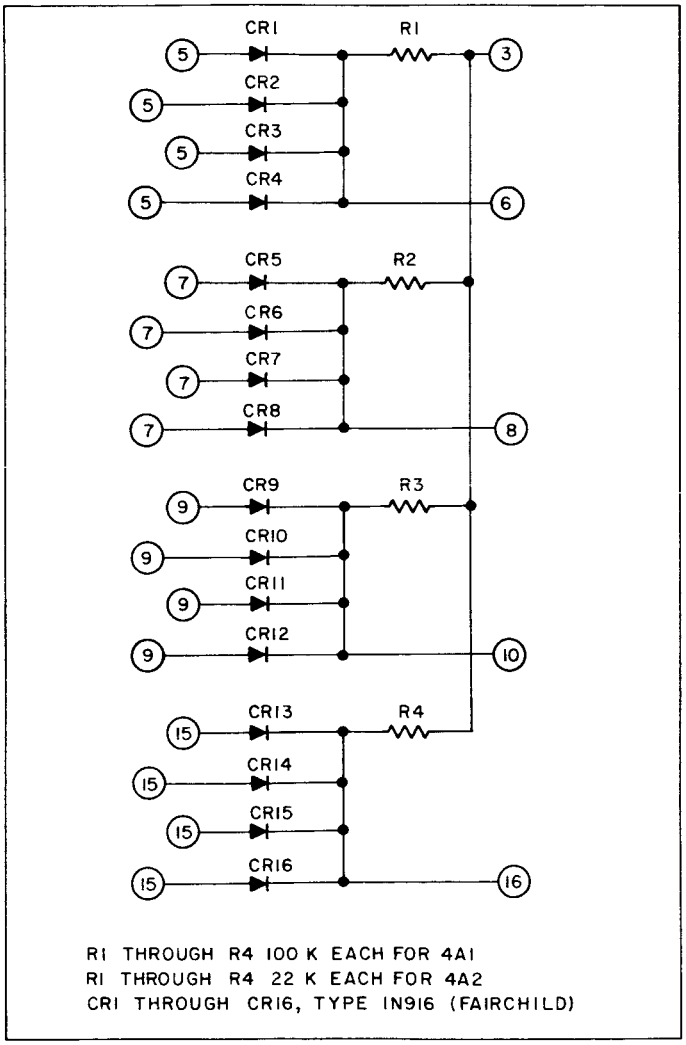


Fig. 59. *And* gate 4 schematic diagram

4. *And* Gate 5

Five 3-legged input *and* gates (Fig. 60) are provided in *and* gate 5. The resistor to 6 v is 22 or 100 kilohms, depending on the output load. The output is normally taken from lead 6. However, where there is not an input diode to the *or* gate, the output is taken from one of the *and* gate input diodes.

5. *Or* Inverter

The *or* inverter circuit (Fig. 61) consists of three diodes *or*ed together at the base of a transistor. Provision for additional gating is made by bringing out the junction of the input diodes which could be wired to the *and* gate diode outputs. The junction of the diodes (lead 6) is connected to the base (lead 7) in the back wiring, either with a direct connection, through a diode, cathode of diode to the base of transistor, or through a 22-kilohm resistor. The connection is shown on the subchassis drawings and depends on the driving source to the *or* inverter. No load resistor is provided on the circuit, and the *or* inverter depends on the external loading for its load. The *or* inverter is also used as a one-shot multivibrator by ac coupling into the base and putting a 22-kilohm resistor to 6 v at that point. When the *or* inverter is used as a one-shot, the input gates are not used.

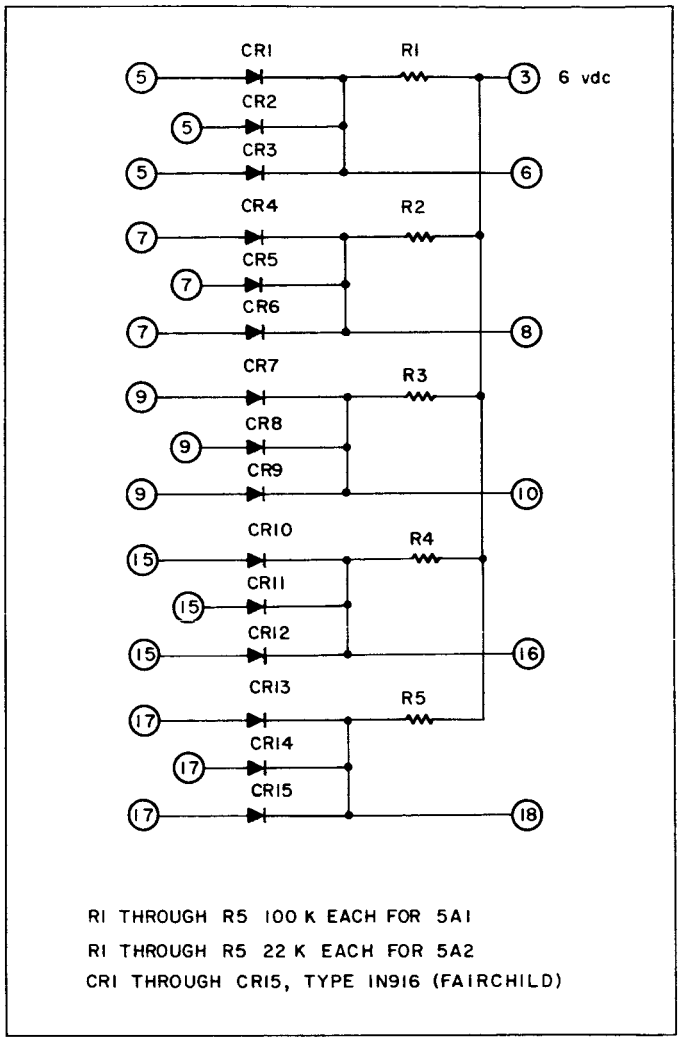


Fig. 60. *And* gate 5 schematic diagram

6. Emitter Follower

The emitter follower shown in Fig. 62 is used when the output of a flip-flop must drive loads to ground. The

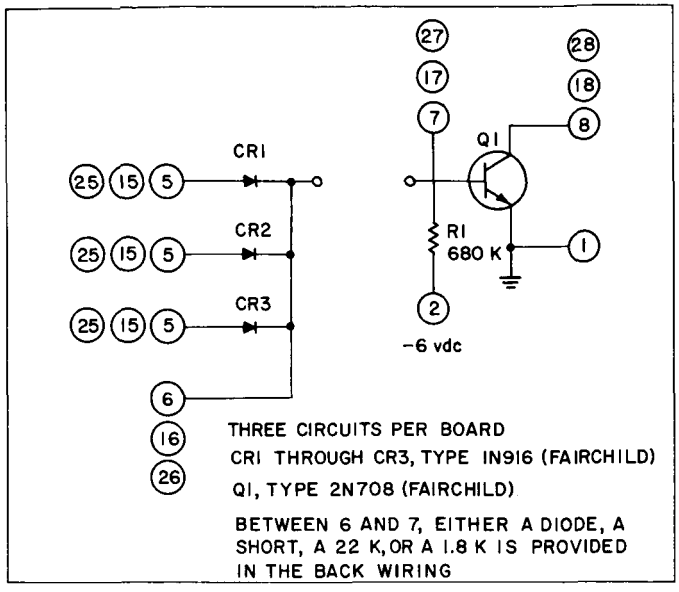


Fig. 61. Or inverter schematic diagram

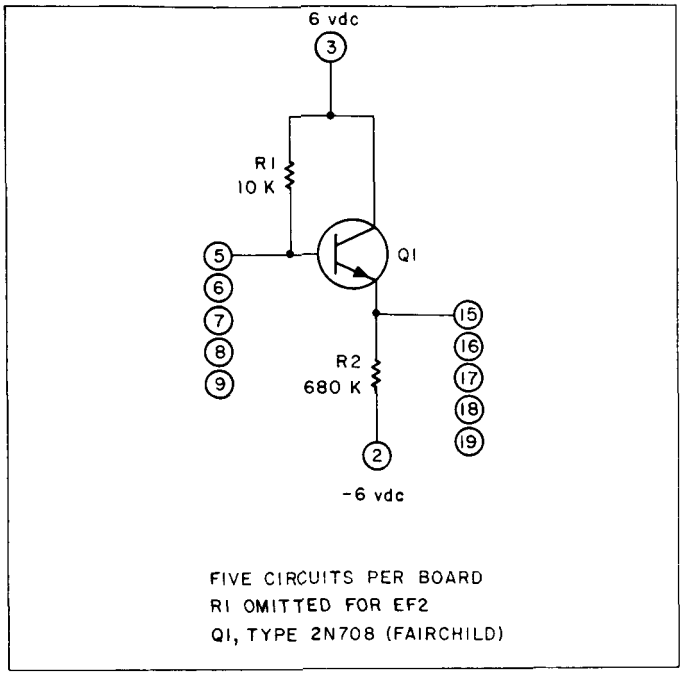


Fig. 62. Emitter follower schematic diagram

680-kilohm resistor, R2, furnishes turn-on current. The remainder of the current is drawn through the load. In some applications, R1 (the 10-kilohm resistor to 6 v) is eliminated since an equivalent resistor is provided in the driving source.

7. 6-Volt Reference Supply

The 6-v reference supply (Fig. 63) is assembled on two modules. The circuit consists of a differential transistor that compares the output of a zener diode against a portion of the output of the reference supply, thus regulating the current through series regulator transistor Q2. Resistor R10 provides a constant load for the reference supply since the current drain from the digital-to-analog converter is a positive current that subtracts from the current through series regulator Q2. Resistors R2 and R6 provide feedback to stabilize the output against input voltage changes. Resistor R3 is the bias resistor for CR1. The value of this resistor is determined by the temperature coefficient of the zener diode and is adjusted as part of the calibration procedure. Resistor R4 is part of dividers R4 and R7; its value determines the output voltage. The value of this resistor is determined at final calibration.

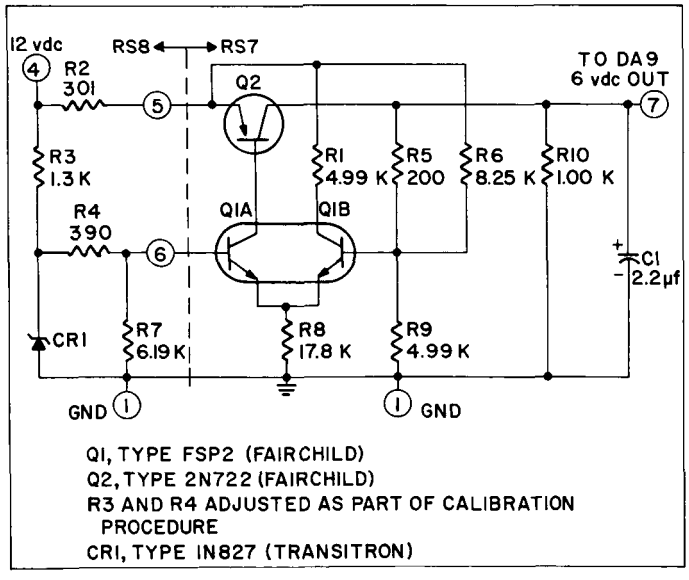
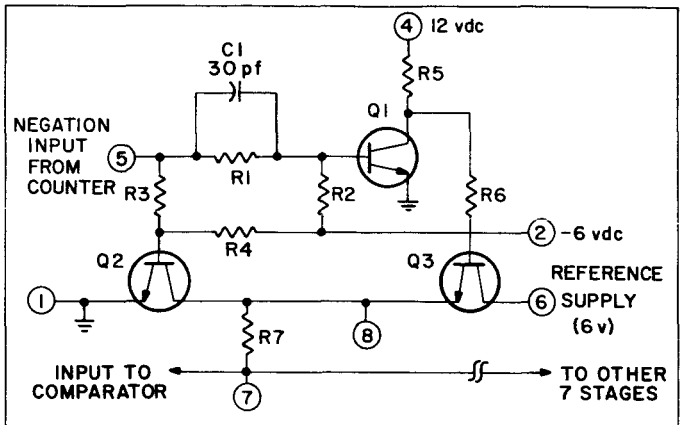


Fig. 63. Reference supply schematic diagram

8. Digital-to-Analog Converter

The digital-to-analog converter (Fig. 64) consists of eight stages of high-accuracy voltage switches tied together through current summation resistor R7. Each stage has two accurate transistor switches, Q2 and Q3, that operate in the supersaturated mode and switch ground or 6 v to point 8. Transistor Q1 is an inverter that guarantees that Q2 and Q3 cannot be on simultaneously. The three most significant stages are designed with a higher level of power than the last five, and with minimizing of the offset voltages of the switching transistors Q2 and Q3. R7 is a fixed precision resistor selected for each stage such that the thevenized voltage at point 7

is an accurate analog representation of the digital inputs from the universal countershift register. If all negation inputs from the counter are positive, all stages of the digital-to-analog converter are tied to ground because of conduction in Q2. A thevenized output voltage of ground exists at point 7. If all negation inputs from the counter are in the zero state, a thevenized output of 6 v exists at point 7. If the most significant digit has a negation input in the zero state, and all other digits have a positive negation input, a thevenized output voltage of 3 v exists.



DESIGN	STAGE NO.	R1	R2	R3	R4	R5	R6	R7	
DA1	(MSD) 1	3.74	53.6	1.62	35.7	4.42	681	5.80	G.I. GPR-5(5/16 h x0.328 DIA.) ASSEMBLED ON LUGBOARD
DA2	2	6.49	100	2.67	53.6	9.09	1.0	11.60	
DA3	3	8.25	100	4.02	53.6	15.4	1.0	23.2	
DA4	4	10.0	100	6.19	100	22.1	1.0	46.4	
DA5	5	10.0	100	6.19	100	22.1	1.0	93.1	IRC MEA
DA6	6	10.0	100	6.19	100	22.1	1.0	187	
DA7	7	10.0	100	6.19	100	22.1	1.0	374	
DA8	(LSD) 8	10.0	100	6.19	100	22.1	1.0	750	

ALL RESISTORS IN K OHMS UNLESS OTHERWISE NOTED
Q2 AND Q3, TYPE 2N771 (FAIRCHILD)
Q1, TYPE 2N708 (FAIRCHILD)

Fig. 64. Digital-to-analog converter schematic diagram

9. Comparator

The analog-to-digital converter comparator (Fig. 65) selects one of twelve input signals by means of an input multiplexer and compares the selected analog voltage with the digital-to-analog converter output.

When transistor Q1 conducts, current flows through R4 if the analog input voltage is greater than the digital-to-analog converter output voltage. Current flows through R5 if the digital-to-analog converter voltage is more positive than the analog input voltage. An equivalent amount of current flows through both resistors if the analog input voltage is equivalent to the digital-to-analog voltage. Twelve identical input comparators compare the twelve input channels against the digital-to-analog converter output. Each input channel has transistors Q1 and Q2. Transistors Q3 through Q8 are shared in common by all analog inputs. Transistor Q1 is a constant-current generator biased on only where the particular channel is selected. Selection is made by gating two matrix inputs. The collectors of all Q2 transistors are tied in common. The digital-to-analog converter is tied in common to Q2B, and a particular analog input is tied to Q2A. When a channel is selected, a constant current, generated by transistor Q1, is shunted from the collector of Q2A to the collector of Q2B as the digital-to-analog input exceeds the analog input; this is amplified by Q3 through Q7. Transistor Q8 is a current switch in the emitters of Q4 and Q5 that allows sampling of the comparator, which guarantees that the digital-to-analog converter input is changed on the leading edge of the 2.4-kc count pulse. The comparator is sampled on the trailing edge of this pulse.

10. Reset Amplifier

The reset amplifier (Fig. 66) is a monostable multivibrator, providing a 4-input ac-coupled *or* gate. A negative transition to one of the inputs turns off Q1, turning on Q2 by the current through R6. The input capacitor discharges through the parallel resistance of R5 and the input gate resistor, causing Q1 to conduct. The output of Q2 is applied as a reset input to flip-flops used in the DAS.

11. Power-On Reset

The power-on reset circuit (Fig. 67) provides a delayed output pulse when power is applied. As the 6-v supply goes positive, Q2 is turned on and Q1 is turned off. When capacitor C1 charges sufficiently to overcome the voltage drop across diodes CR2, CR3, and CR4, Q1 conducts. During this time (15 millisec), C2 charges through resistor R7 to a voltage determined by dividers R7 and R8. As Q1 is turned on, Q2 turns off, applying positive voltage to the collector of Q2 and providing regeneration through R9 and C4 to the base of Q1. This results in a fall time of less than 1 μsec at the output. The negative-going output triggers the reset amplifiers, resetting the DAS.

L. The Power Supply

The DAS transformer/rectifier unit is a solid-state rectifier and voltage regulator that provides the operating

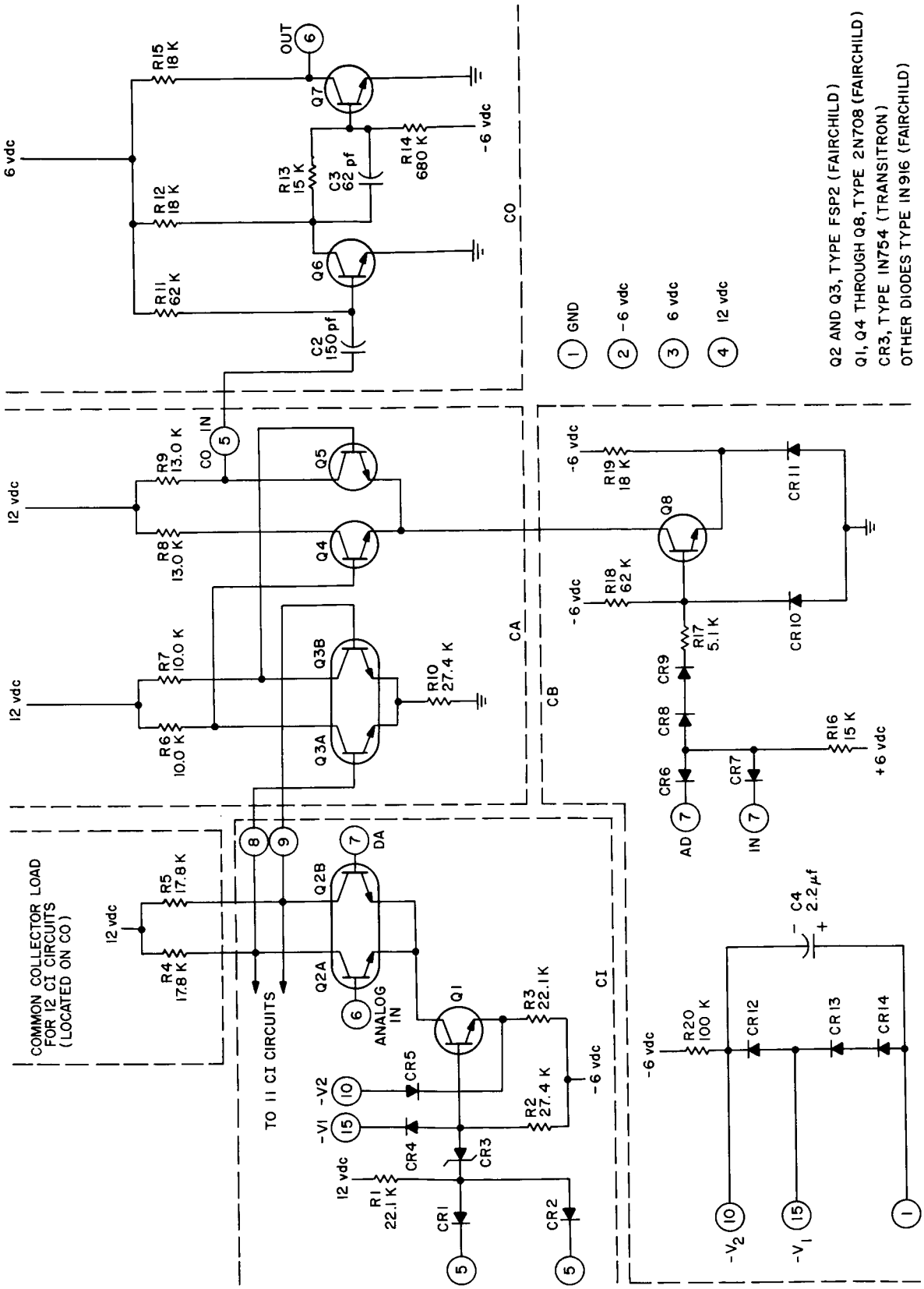


Fig. 65. Comparator schematic diagram

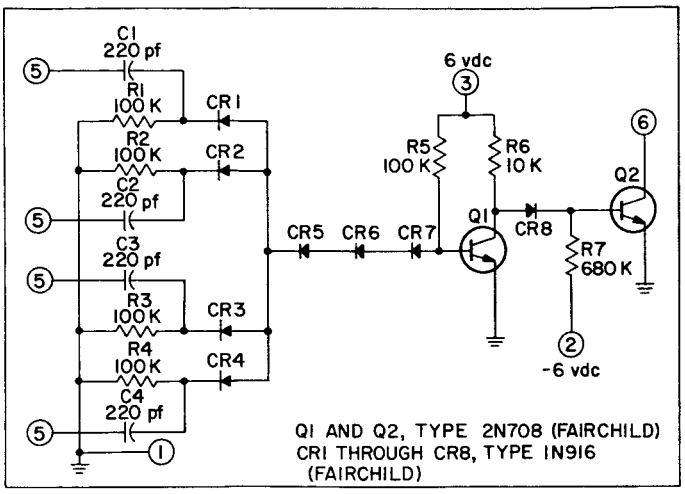


Fig. 66. Reset amplifier schematic diagram

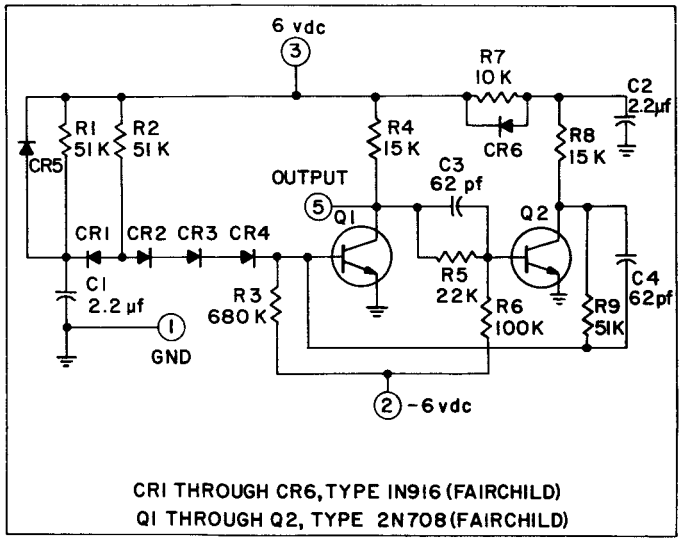


Fig. 67. Power on reset schematic diagram

voltages to the DAS. This unit contains three dc voltage regulators that supply 12, 6 and −6 v. Figure 68 is a schematic of the DAS transformer/rectifier unit.

The input to the TR unit is a 26-v rms squarewave at 2400 cps. The outputs are as follows: 12 vdc at 35 milliamp, 6 vdc at 150 milliamp, and −6 vdc at 15 milliamp. The regulation of the dc voltages is 2% with a peak-to-peak ripple of 1%.

Each regulator operates the same, the only difference being the circuit values. Referring to Fig. 68 and using the 12-v regulator as an example, the stepdown 2400 cps is rectified by CR1 and CR2 and applied to the filter L1 and C1. This voltage is 6 v and is used as a reference supply for the amplifiers and the regulator.

The voltage on the second winding is rectified by CR3 and CR4 and filtered by L4 and C2. This is the main power source for the 12-v regulator and is about 13 v at full load.

Transistors Q5 and Q6 are used as a differential amplifier to sense the output voltage variations. The base of Q5 is clamped at a reference of 5.6 v by CR20, and the base of Q6 is adjusted by the values of RX to obtain an output of 12 v. If the output voltage tends to increase, more base current flows in Q6. As the result of increased base current, a collector current of βI_B causes a drop of Q6 collector voltage. This drop causes an identical voltage rise of collector Q5. This potential rise is dc-coupled by CR19 to the base of Q13 and causes a drop in collector current. CR14 holds the emitter of Q13 at a constant voltage of 3.3 v below the output voltage.

The drop in Q13 collector current allows the base of Q4 to go more negative and tends to turn Q4 off. Since the series regulator Q1 is a cascade emitter follower, it also turns off, thereby reducing the original output voltage increase.

The series combination of CR13 and R7 supplies sufficient current at power-on to turn Q1 on. R2 and C9 provide a negative ac feedback path to suppress any oscillation which may be caused by load changes.

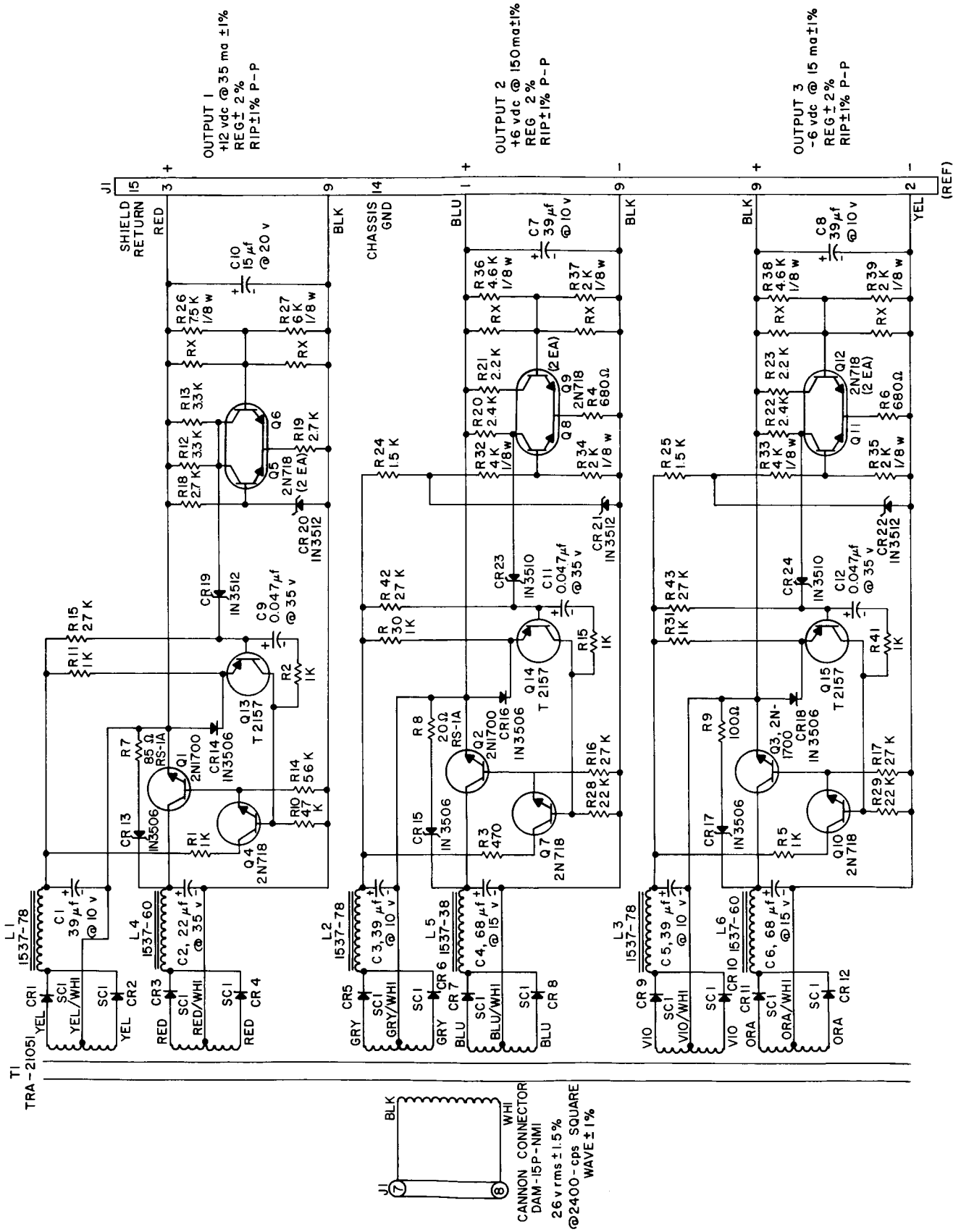


Fig. 68. Data automation system power supply schematic diagram

XIV. SCIENTIFIC GROUND SUPPORT EQUIPMENT

The Ground Support Equipment (GSE) for *Ranger* Follow-On scientific instrumentation, when operated in conjunction with appropriate stimuli applied to the instrument, provides an overall check on instrument performance. Both visual monitoring of outputs and a hard copy printed record of test results are provided. In addition, GSE is able to monitor and print out on paper tape a record of all power-supply voltages present in the scientific instrumentation subsystems. External stimuli are required by each experiment in order for all experiment components to function normally. Except for radiation sources, all appropriate stimuli for the experiments are controlled by the GSE. In all cases except one, stimuli injection is provided directly to the input of the experiment. To provide a more complete test of experiment operation, the GSE is also able to give commands and monitor outputs from the experiments which are not monitored during flight. In general, the purpose of the GSE checkout procedure is to establish a go/no-go condition of the equipment rather than to check the absolute calibration of each experiment in terms of the physical units being measured. Such absolute calibrations will have been performed by the individual scientific experiment groups prior to installation on the vehicle. Physically, the scientific GSE consists of two equipment racks. Although separate patch boards are provided for each experiment for greater flexibility, a system patch board will provide the proper interconnections to check out each experiment individually or all experiments at the same time.

A. *Stimulus and Response*

The following stimuli are applied to the various instruments, with the responses as indicated.

1. **Particle flux detector (unit 20A3) and Neher ion chamber (unit 20A2)**

   Stimulus: A cobalt-60 radioactive source located on the spacecraft close to the Neher ion chamber.

   Response: Visual indication at a counter in rack 20A2 automatically sampled for a predetermined time and tape printout.

2. **Electron flux detector (unit 20A13)**

   Stimulus: An alpha and beta radioactive source mounted on the sensor input.

   Response: Visual indication at a counter in rack 20A2 automatically sampled for a predetermined time and a tape printout.

3. **Cosmic dust detector (units 20A16, 20A19/10, and 20A10/19)**

   Stimulus: Commands from rack 20A1 to a mechanical actuator mounted on each sensor.

   Response: Tape printout from rack 20A2.

4. **Search coil magnetometer (units 20A11 and 20A17)**

   Stimulus: High-scale, IFC-off, and IFC-on commands from rack 20A1.

   Response: Visual indication at a DVM and tape printout of DVM reading from rack 20A1.

5. **Electron-proton spectrometer (units 20A14 and 20A18)**

   Stimulus: A cesium-137 radioactive source and polonium-210 radioactive source located on the spacecraft close to the sensor of the EPS. A sequence command is also provided from rack 20A1.

   Response: A visual indication at a DVM and tape printout of DVM reading from rack 20A1.

6. **Low-energy plasma probe (unit 20A15)**

   Stimulus: (a) A binary drive command from rack 20A1
   (b) A binary lock command from 20A1
   (c) Voltage steps to simulate electrometer current from rack 20A1

   Response: Visual indication at a DVM and tape printout of DVM reading from rack 20A1.

7. **Low-energy ion detector (unit 20A12)**

   Stimulus: A timing command from rack 20A1 and current injection to the input of the electrometer by using a precision variable voltage source at rack 20A1 and a high-value precision resistor.

   Response: (a) Visual indication at a DVM and tape printout of DVM readings from rack 20A1.
   (b) A visicorder printout of the commutation position of the low-energy ion detector.

B. Description of Equipment

A block diagram of the physical location of each of the components that make up the racks is shown in Fig. 69. Figure 70 is a photograph of the equipment. Automatic features were built into the GSE to reduce the manual operations required and facilitate the operation of all three racks by one operator. A brief functional description of the components in the scientific GSE is as follows:

1. Digital Voltmeter (Non-Linear Systems,[1] Model V34A)

This DVM is used primarily to monitor analog voltages from the spacecraft and provide the NLS digital recorder Model 155 with print information and a print command. The scan and print cycle is remotely controlled from the analog selector panel.

2. Digital Voltmeter (Non-Linear Systems, Model V35B)

This DVM is used to monitor dc voltages from both the spacecraft and the GSE. It also provides the NLS digital recorder Model 155 with print information. The scan and print cycle is remotely controlled by the voltage scanner.

3. Digital Comparator (Non-Linear Systems, Model 55)

Voltages monitored by DVM V35B are also compared with programmed voltage tolerances by the digital comparator. When an out-of-tolerance condition is detected, a command is sent to the voltage scanner which gives a light indication showing which voltage is out of tolerance. This same out-of-tolerance command is used by the NLS digital recorder to give an out-of-tolerance printout (*) next to the appropriate voltage.

4. Voltage Scanner

The V35B DVM, the voltage comparator, the NLS digital recorder, and the voltage scanner were designed to work together as a system, the voltage scanner being the heart of the system. Front panel controls include a reset command which resets the stepping switch to the home position, a manual/automatic mode select which selects the stepping command source used for the stepping switch, a start command which begins the automatic stepping sequence by moving the stepping switch from its home to its first position, and a manual advance command that manually steps the stepping switch when in the manual mode.

A typical logic sequence is demonstrated with the use of the block diagram in Fig. 71. (Also see photograph, Fig. 72.) Assuming that the voltage scanner is in the automatic mode and the stepping switch is in any one definite position, a dc voltage is connected to the DVM input by the stepping switch via the override logic. If the ripple component of the dc voltage is great enough so that the DVM will not stabilize in 10 sec, the override logic will inhibit the dc voltage and short the DVM inputs together in order for the scanning cycle to continue. After the DVM has stabilized, a decimal representation of the input voltage is presented to both the comparator and the printer, and a DVM print command is issued to the comparator. The DVM print command momentarily connects the start trigger lead to the comparator's ground lead, which starts the comparison process. The high and low comparator tolerance have already been programmed by the stepping switch which grounds the proper high and low comparator tolerance pins with the use of a diode matrix.

At the end of the comparison process, the comparator issues a print command to the printer, which prints the following three bits of information:

1. The dc voltage being displayed by the DVM.
2. An asterisk if the input voltage is out of tolerance or a blank if it is not.
3. The step position of the stepping switch.

If an out-of-tolerance condition is realized, the following sequence of events occurs:

1. The comparator provides a relay closure at the same time the print command is issued.
2. The print command is routed through the relay contact to the go/no-go logic and drivers.
3. A print command is issued to the printer for an asterisk printout and also to a latching relay which turns on the channel number indicator light on the front panel. After the print cycle is complete, the printer issues a print-complete command to step the stepping switch to the next position and to issue a DVM scan command.

The start reset and manual mode logic has three functions.

1. For manual operation, the mode select switch inhibits the printer print-complete command and connects the manual advance switch to the driver logic. In this configuration, the stepping switch can be manually advanced from the front panel. This action is reversed for automatic operation.

[1]Non-Linear Systems, Inc., Del Mar, Calif.

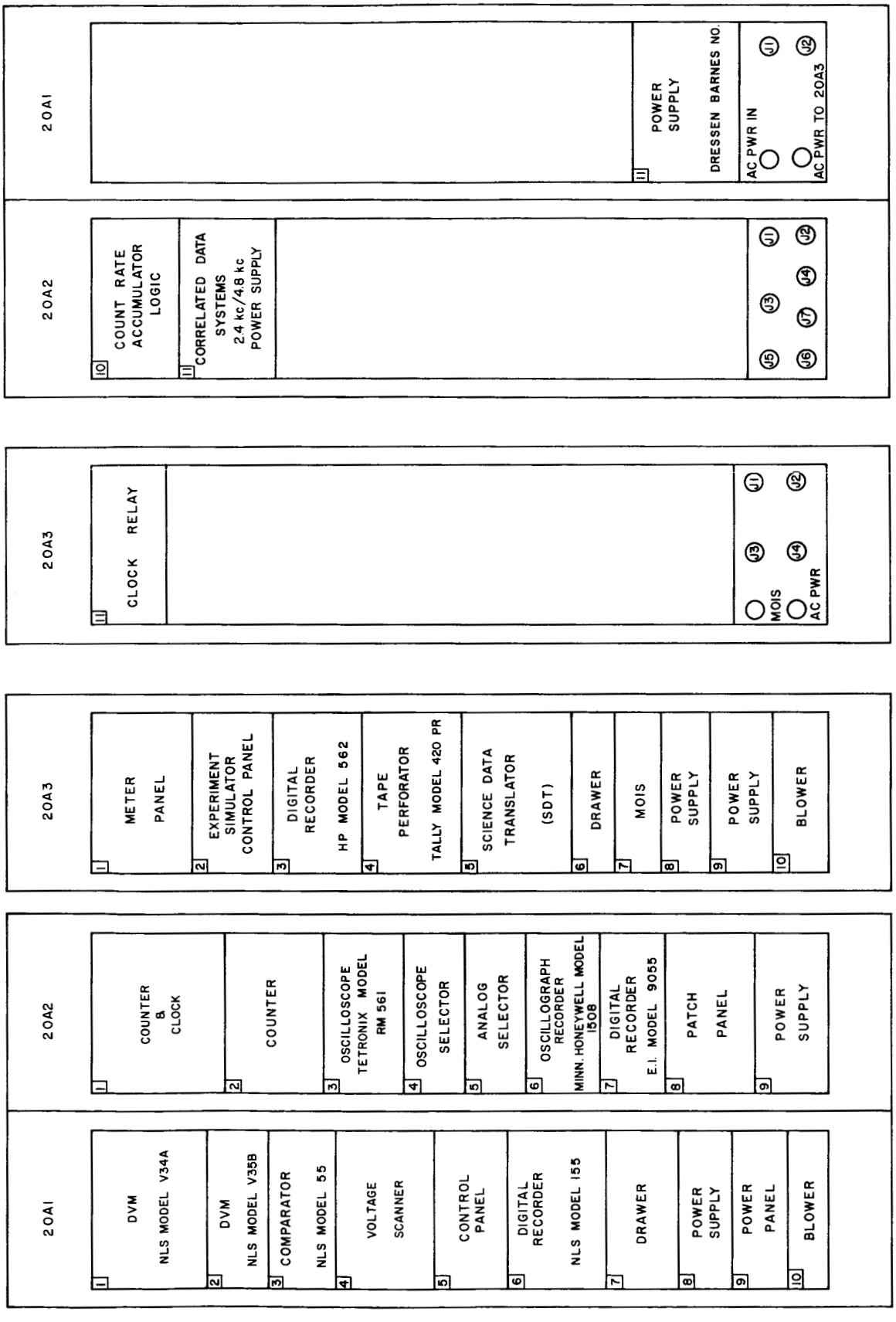


Fig. 69. Rack assembly, *Ranger* Follow-On, science GSE

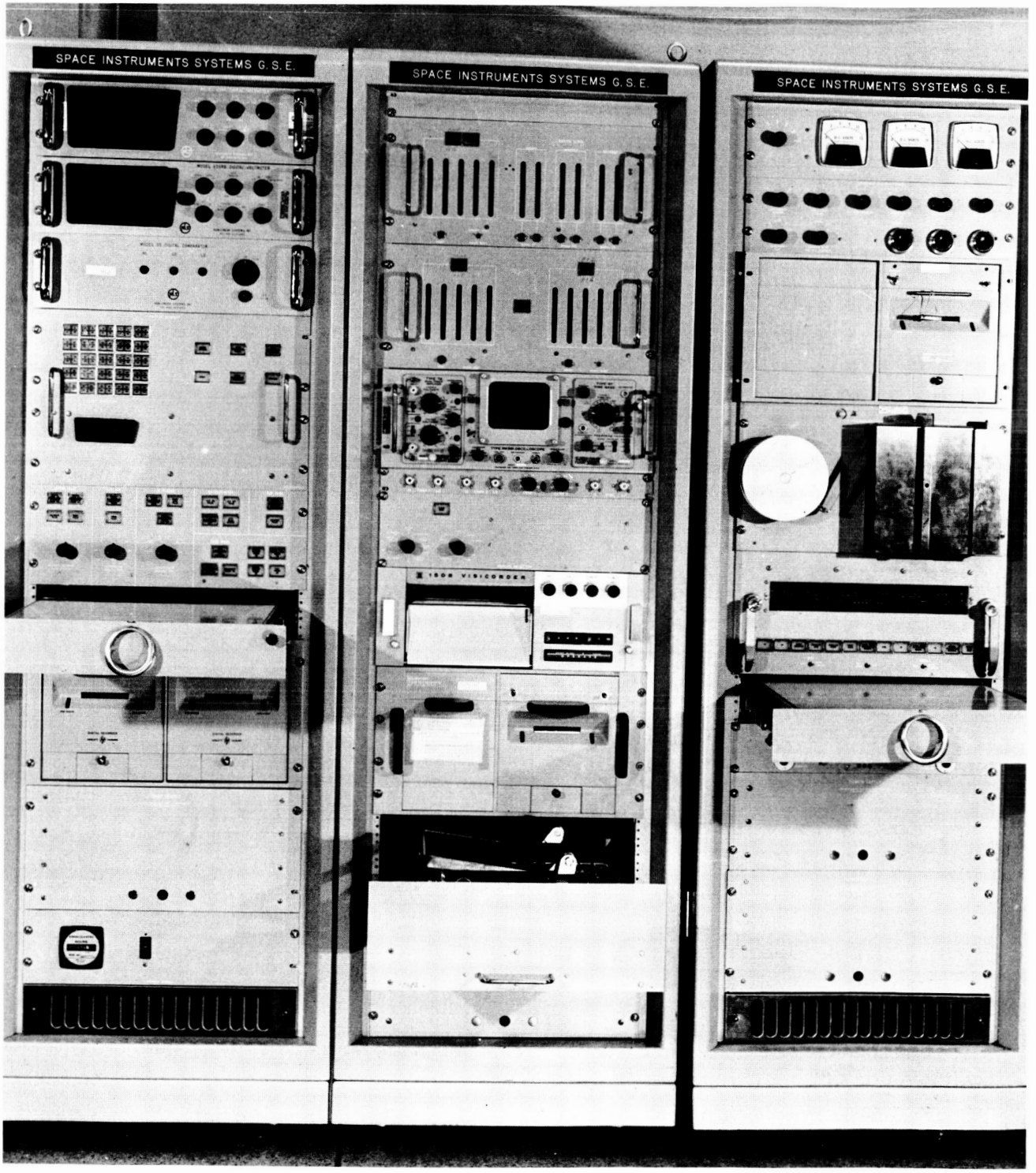


Fig. 70. *Ranger* Follow-On science GSE

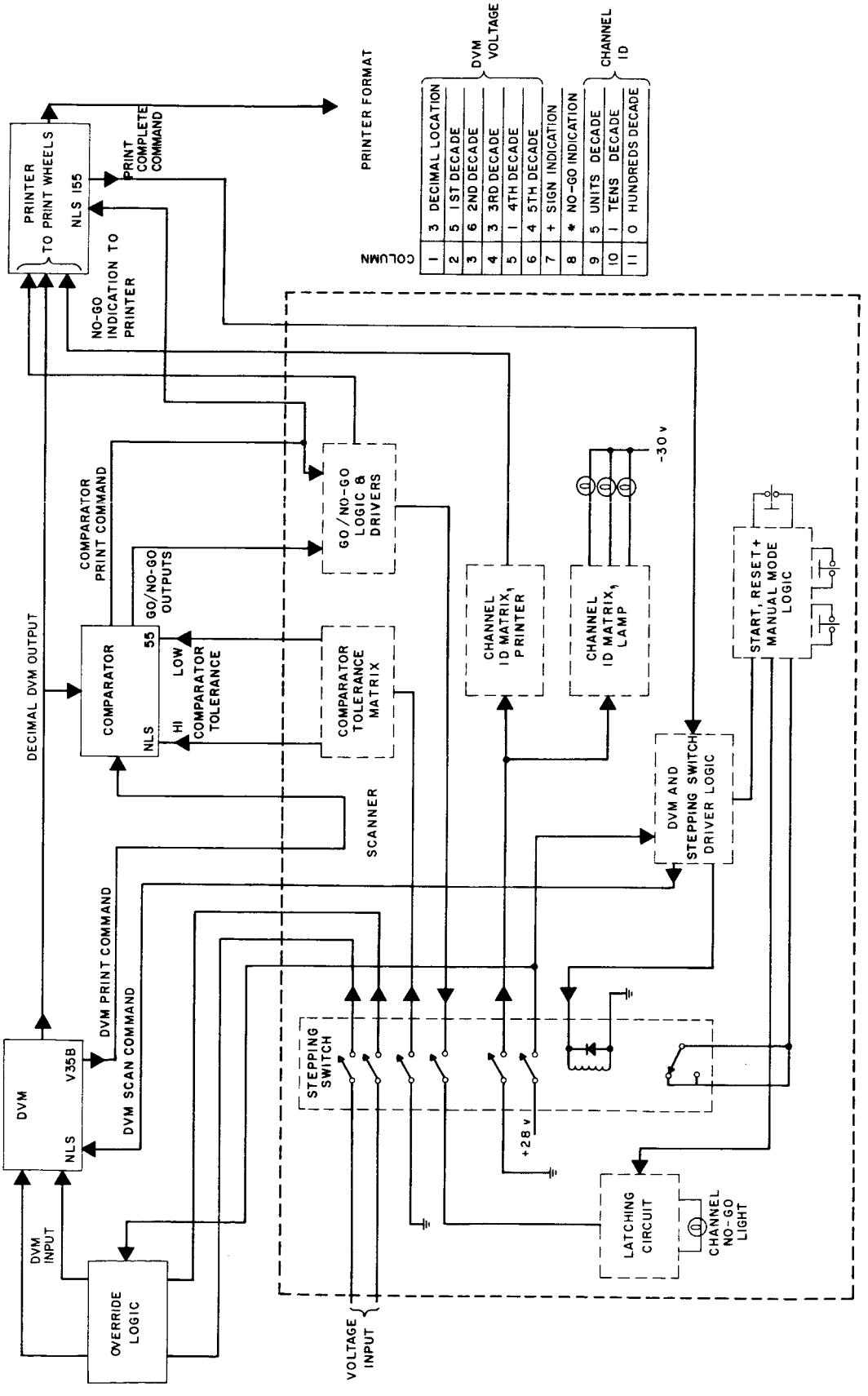


Fig. 71. Voltage scanner block diagram

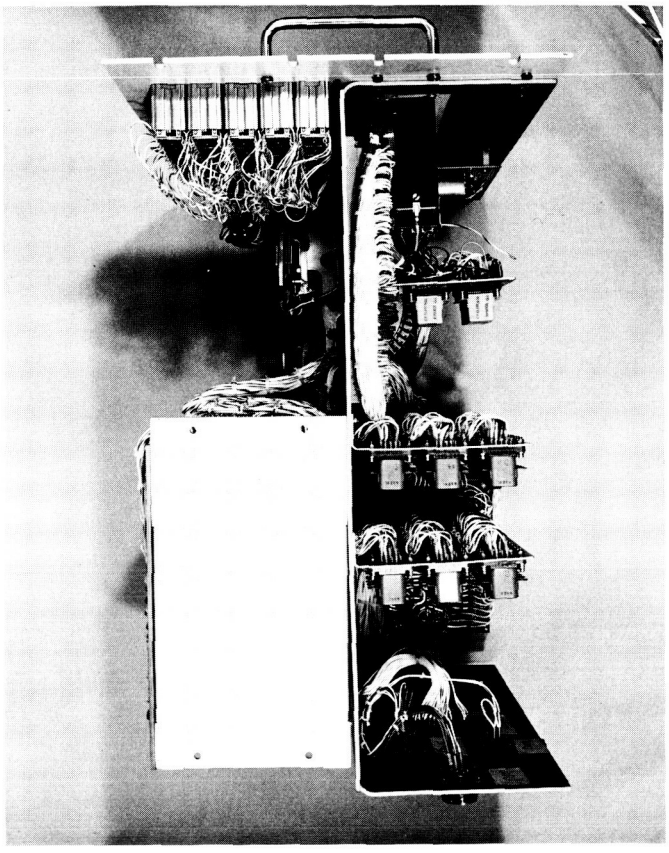


Fig. 72. Voltage scanner

2. A reset command drives the stepping switch to its home position and provides an unlatching voltage to the channel indicator out-of-tolerance lights relays.

3. The start command steps the stepping switch from its home to its first position and is then inhibited.

When the voltage scanner operates in the automatic mode, it is a simple matter to obtain a printout of all the dc voltages monitored during any phase of the check-out procedure.

5. Control Panel

GSE control panel in rack 20A1 provides control of spacecraft monitoring and GSE command circuits. A brief functional description of the control panel is as follows:

1. Automatically provides the proper stimulus and a visual indication of that stimulus for the low-energy plasma, low-energy ion, and cosmic dust experiments.

2. Controls the primary power used for the power supplies of the count rate accumulator, voltage scanner, science data translator, and control circuits.

3. Simulates the DAS command functions to the cosmic dust, low-energy ion, low-energy plasma, magnetometer, and electron-proton spectrometer experiments either automatically or manually.

4. DAS or GSE source of commands to the experiments can be selected.

5. Provides external power to the spacecraft TR or inverter units when spacecraft power is not available.

6. The low-energy plasma binary lock and magnetometer high scale commands can be given by push-button controls which also provide an illuminated indication of which controls are in use or can be used by the operator.

The control panel and isolation box should be considered as one unit, since all the experiment command functions from the control panel are routed through the isolation box to the individual experiment. Figure 73 demonstrates the system flow for command generation by the GSE.

In a typical command sequence with the command source select in the GSE command position, the relay contacts in the isolation box are as shown. Automatic pulse logic using flip-flops and amplifiers was designed to simulate the command repetition rate from the DAS to the experiments. In some cases it was desirable to send commands to the experiment at a repetition rate convenient for a more thorough investigation of a particular experiment's reaction to that command. A manual trigger one-shot is used for this purpose. Automatic or manual commands are selected by the mode select and sent to a pulse shaper in the isolation box. The output of the pulse shaper then goes to the experiment and also through an isolation amplifier back to the GSE for monitoring purposes. With the command source select in the DAS command position, the pulse shaper is disconnected and commands initiated by the GSE no longer have any effect. Since the isolation amplifier is still monitoring the input command lines to the experiment, all commands initiated by the DAS are available for monitoring at the GSE.

The cosmic dust command logic functions in the same manner as that just described. The monitored reset pulse is delayed and used as the trigger for six one-shots. Three

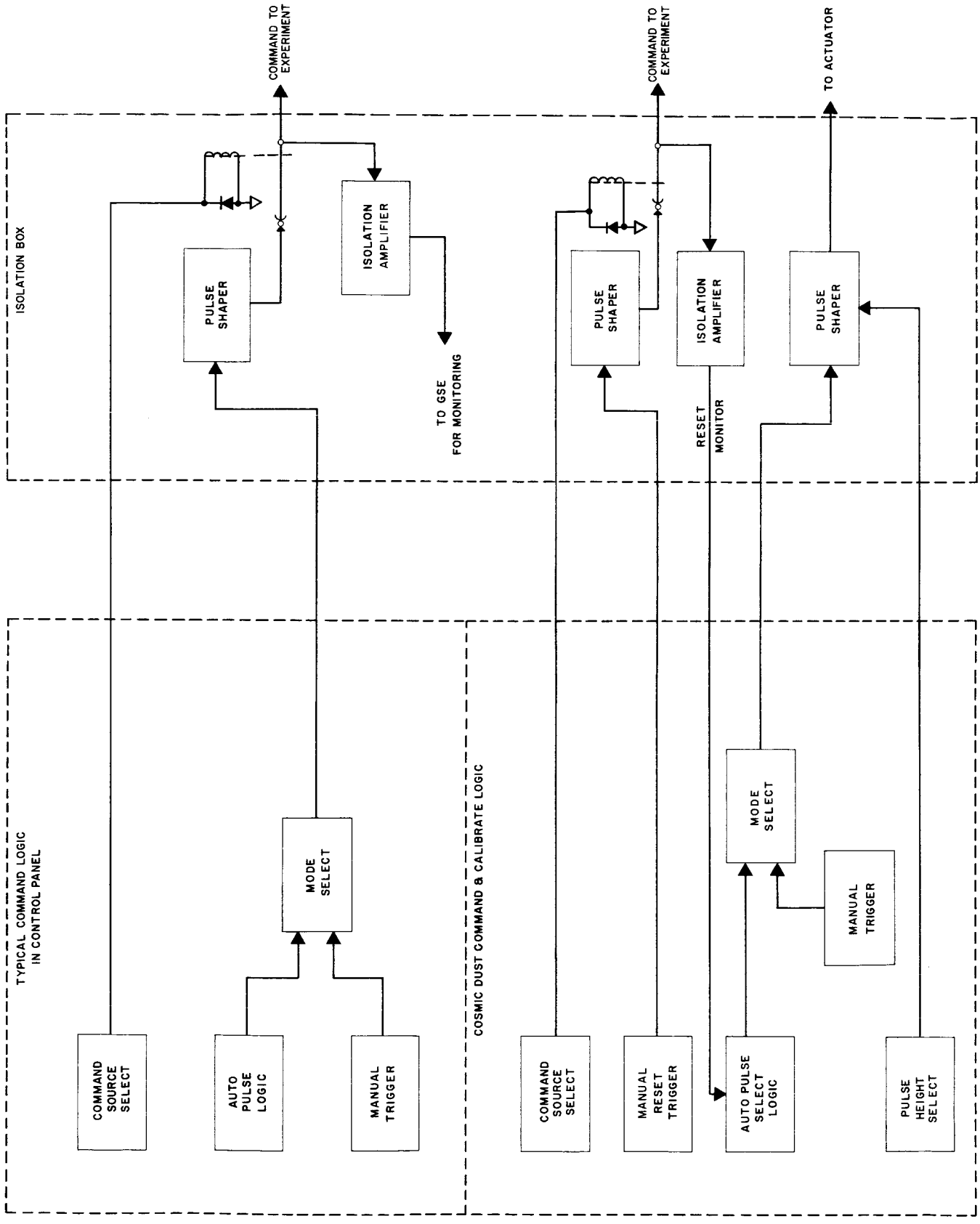


Fig. 73. Control panel block diagram

calibrate pulses are generated by this logic. The number of pulses to be used is determined by the position of the selector switch. A manual trigger one-shot is also provided here for the same purpose as previously mentioned. The calibrate pulse source is selected by the mode select, sent to the isolation box pulse shaper, and from there to a mechanical actuator located on the sensor plate of the cosmic dust experiment. The pulse height selector determines the amplitude of the calibrate pulse used to trigger each actuator.

With the proper selection of switches, it is relatively simple to automatically provide experiment stimulus and automatically simulate DAS commands. This versatility allows the operator to concentrate his efforts on data evaluation rather than equipment operation.

6. Digital Recorder (Non-Linear Systems, Model 155)

Printer 1 is used with the voltage scanner system and records dc voltages from the spacecraft and the GSE. Printer 2 is used primarily to record analog voltages from the spacecraft.

7. Power Supplies (Dressen-Barnes[2])

GSE unit 20A1-8 contains three power supplies used for the count rate accumulator. They are:

1. −11 vdc, Model 22-213.
2. +6 vdc, Model 20-6.
3. −18 vdc, Model 25-411.

GSE unit 20A1-11 contains six power supplies used for the following applications:

1. +12 vdc, Model 30-12. Used for GSE command and control circuits.
2. −12 vdc, Model 30-12. Used for GSE command and control circuits.
3. +50 vdc, Model 10-55. Used for GSE command and control circuits.
4. −30 vdc, Model 10-30. Used for the count rate accumulator, voltage scanner, and command circuits.
5. +18 vdc, Model 20-18. Used for the count rate accumulator.
6. −9 vdc, Model 10-30. Used for the spacecraft inverter.

[2] Dressen-Barnes Electronics Corp., Pasadena, Calif.

8. Count Rate Accumulator and Clock

The count rate accumulator (CRA), clock, and the EI digital recorder were designed to function together as a system with the following capabilities:

1. The accumulation and printout of digital data from the particle flux, electron flux, and ion chamber experiments.
2. The accumulation and printout of binary information from the cosmic dust experiment.
3. Provision of accurately timed pulses to other subsystems in the GSE such as the clock relay chassis and the control panel.

Three 5-decade counters are utilized to display the digital outputs of the particle flux and electron flux experiments and present the EI digital recorder with a BCD representation of the digital number. Three of the seven outputs are accumulated for 1 min and are then presented sequentially to the EI digital recorder for printout. Because of the low pulse rate, ion chamber pulses are displayed on the EI recorder as event time. Since the occurrence of ion chamber pulses is not predictable, the presentation of these data to the EI recorder takes precedence over cosmic dust data. Every 40 sec the cosmic dust experiment binary output is sampled and presented to the EI digital recorder as a 6-bit binary word. A brief logical description of this system will be given using the CRA logic diagram shown in Fig. 74. (Also see photograph, Fig. 75.)

The major portion of components used in the CRA logic are EPSCO transistor plug-in units. Eight Computer Measurement Company[3] decades are used in the clock pulse generator section. At the extreme right of the logic diagram a 2.4-kc squarewave from the GSE rack supply is coupled through a transformer for ac isolation and amplitude reduction. The 2400-cps squarewave is then current-amplified, divided by 6, current-amplified again, with the resulting 400-pps signal sent to the control panel and through two more flip-flops. The 100-pps signal is divided to 10 pps, 1 pps and 1 pulse per 10 sec by CMC decades. The 2 and 4 BCD outputs from the 10-sec decade are *and*ed together to a 14-μsec one-shot which sends 1 ppm to the master timer circuit at the extreme left and is also amplified and used to reset the 10-sec decade when it has reached 60 sec. The 1-min, 10-min,

[3] Computer Measurement Co., Div. of Pacific Industries, San Fernando, Calif.

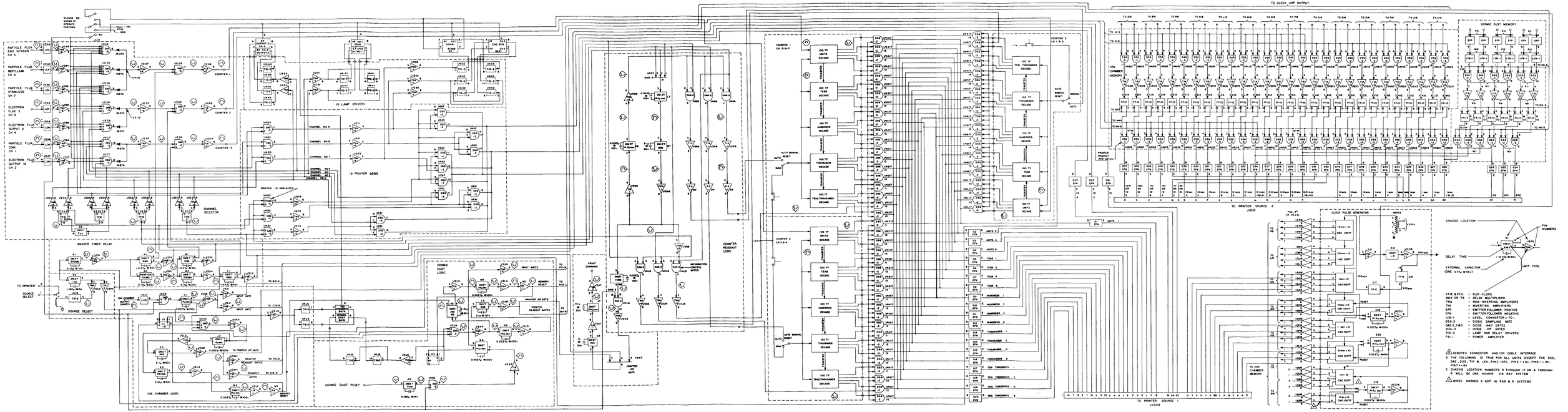


Fig. 74. Count rate accumulator logic diagram

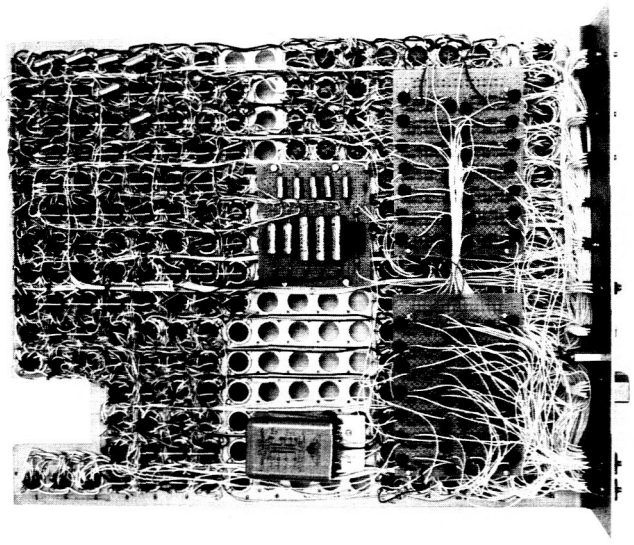


Fig. 75. Count rate accumulator

1-hr, and 10-hr decades are actuated in the same manner. The BCD outputs from all the decades are amplified and sent to the clock relay chassis and to the input of all the ion chamber memory *and* gates. The remaining source for these *and* gates will be described as the logic sequence continues, and for clarity, the remaining description will be broken down into three different types of inputs; ion chamber, cosmic dust, and digital. All three types of inputs are located at the extreme left of the logic diagram.

a. Ion chamber input. The positive ion chamber pulse is first level-converted to a negative pulse to mate with the EPSCO logic and sent to an *and* gate. The remaining input of this *and* gate comes from the operate standby switch and is at a true (or logic one) level (−6 v) when in the operate mode. This output triggers a 14-μsec one-shot which has two outputs. One output is amplified twice and provides the remaining input required to open the ion chamber memory *and* gates. In the ion chamber memory, time in BCD form is amplified and sets the memory flip-flops which provide one of the inputs to the printer readout *and* gates. The second output of the input one-shot sets a flip-flop which provides a true level to the ion chamber *and* gate and a false level to the cosmic dust *and* gate.

One of the remaining inputs of the ion chamber *and* gate comes from the source select one-shot which provides a false level one time per minute when the source select is in position 1. This ensures that the diode gate will not be activated when the printer is in the incorrect source. The remaining *and* gate input comes from the cosmic dust one-shot which provides a false input from the cosmic dust one-shot for 250 millisec if cosmic dust data have been entered into the logic and that printing cycle has begun. The flip-flop output to the *and* gate also goes through an amplifier feeding two relay drivers which turn on the ion chamber data indicator light.

The *and* gate output is amplified and triggers a 3 millisec and 250-millisec one-shot. The 3 millisec one-shot is used as a delay to allow information settling time in the ion chamber memory. The signal from the 3 millisec one-shot is amplified and triggers a 5-millisec one-shot, is again amplified and used to provide the second input to the printer readout *and* gates. BCD time is then presented to the printer through emitter followers. The output of the 5-millisec one-shot amplifier is also sent to the printer *or* gate, where it is delayed 1 millisec by a one-shot to allow information settling time in the printer, amplified, and used to trigger a 300-μsec one-shot which sends a print command through an amplifier to the printer.

Return to the point where the diode *and* gate output has been amplified and used to trigger a 250-millisec one-shot. This one-shot is used as a delay to allow the print cycle to be completed. The output signal is then amplified, used to trigger a 14-μsec one-shot whose signal is then amplified and sent both to the ion chamber memory to reset the storage flip-flops and is also used to reset the first flip-flop that was set by the incoming ion chamber pulse. From the above description, it can be easily seen that the ion chamber data and the cosmic dust data pulse are both stored in flip-flops, which in turn are controlled by *and* gates. Therefore, this information cannot be lost, but only momentarily delayed until all other logic cycles have been completed.

b. Cosmic dust input. Cosmic dust information enters into this logic as six discrete 0– or 6–v levels. These inputs are located on the block diagram just to the right of the ion chamber memory. This signal is brought through an emitter follower for current amplification, level-converted, and then used for one input of the first diode *and* gate in this particular logic string. The cosmic dust reset (just to the right of the ion chamber logic in the lower left-hand corner of the block diagram) pulse is first delayed for 3 sec to allow information to be stored in the cosmic dust experiment, flows through the *and* gate which is controlled by the operate standby switch, is amplified and used to trigger a 14-μsec one-shot. One

output of this one-shot is then amplified and used as the second input to the first diode *and* gate in the cosmic dust experiment memory.

The output signals from these *and* gates are then inverted, amplified, and used to set the six storage flip-flops. The outputs of the storage flip-flops are presented to one input of the printer readout *and* gates. The second output of the 14-μsec one-shot sets a flip-flop. The true level output from the flip-flop is first amplified and then used as an input to two relay drivers which turn on the cosmic dust data indicator light. The same flip-flop output is used as one input to a diode *and* gate. The second input to this diode *and* gate comes from a similar flip-flop in the ion chamber logic. If ion chamber data have not been entered into the logic, this input is at a true state. However, if ion chamber data have been entered into the logic, this input will be false, holding the *and* gate off. The last input of this *and* gate is controlled by the 1-ppm source select one-shot input. If the digital data cycle has begun, the same 1-sec pulse which held off the ion chamber *and* gate also keeps this *and* gate in the off position until the digital data cycle has been completed.

If all the *and* gate inputs are true, the output level is amplified and used to trigger a 3-millisec one-shot and a 250-millisec one-shot. One of the 250-millisec one-shot outputs is returned to the ion chamber *and* gate, holding it off until the cosmic dust print cycle has been completed. Explanation of the second output of this one-shot will be delayed for reasons which will become obvious. The output of the 3-millisec one-shot is first amplified, then used to trigger a 5-millisec one-shot whose output is again amplified and then used to initiate two logic reactions. The output pulse goes to the printer *or* gate, where print command is finally produced in an identical manner as was described for the ion chamber logic. This same 1-millisec pulse is used as the second input to the printer readout *and* gates in the cosmic dust memory. Cosmic dust information is then presented to the printer in the same manner as were the ion chamber data. The second output of the 250-millisec one-shot is amplified and used to trigger a 14-μsec one-shot whose output is inverted and again amplified. This signal resets the cosmic dust memory flip-flops and also resets the first flip-flop after the 14-μsec one-shot in the reset pulse logic. Sequencing of the cosmic dust experiment logic is now complete.

c. Digital input. All of the 0- to 6-v pulse inputs (located at the upper lefthand corner of the block diagram) are level-converted, amplified, and used as one input of a diode *and* gate. The remaining inputs for these *and* gates (numbered 1 through 7 from top to bottom) will be explained first. Two of the remaining inputs for *and* gates 1 through 3 and one of the remaining inputs for *and* gates 4 through 7 are controlled by the operate/standby switch. All remaining *and* gate inputs are derived from the channel selector flip-flops. One ppm from the clock triggers a 1-sec one-shot and 250-millisec one-shot. The output of the 1-sec one-shot blanks off the ion chamber and cosmic dust *and* gates and also drives a relay driver, which in turn actuates a relay that changes the printer source from the normal No. 2 position to the No. 1 position. The 250-millisec signal triggers an 8-millisec one-shot and a 250-millisec one-shot through an amplifier. One output of the 8-millisec one-shot is amplified and produces a pulse which will be called pulse A. Pulse A sets flip-flop 1 in the channel selector, which in turn sets flip-flop 2. The true outputs of these two flip-flops are amplified and provide the remaining two inputs required by No. 1 *and* gate. No. 1 gate is the only gate open of the first three, and the output signal is amplified and used as one of the inputs to the counter *and* gate.

Pulse A also activates an *or* gate in the counter readout logic, which triggers a 3-millisec one-shot. This output is amplified and:

1. Produces a print command as was previously described.
2. Is again amplified and provides one input back to three of the printer ID *and* gates and at the same time provides one input to the information control gates, with the other input being pulse A. The output of this control gate is amplified and used as one of the two counter No. 1 *and* gate inputs. Digital information from the decades is the remaining input to these gates. These gates provide information to the printer as was previously described.

The trailing edge of the 3-millisec amplified pulse triggers a 14-μsec one-shot, which is then amplified and used as one input to the reset *and* gates. Pulse A is a remaining input to this gate. The output of this gate is amplified and resets counter 1. Pulse A is also used as the second input to the printer ID *and* gate. This output is amplified and again fed to one side of an additional *and* gate. The remaining input source to these gates is derived from the channel selector flip-flop outputs. With channel selector flip-flops 1 and 2 in the position previously stated, only channel 5 buffer *and* gate will be turned on, which will provide the second input to the *and* gates fed by the printer ID *and* gates. The output of these gates is presented to the printer as a BCD numeral 5 for channel identification printout.

The second output from the 8-millisec one-shot in the timer delay logic is used to hold the counter *and* gate off to allow completion of the cycle just described. The second 1-ppm signal from the clock sets flip-flops 1 and 2 in a channel selector to a 0110 logic position. This opens the second input gate for counter 1, and the cycle repeats. The third input pulse from the clock sets flip-flops 1 and 2 to a 1010 logic position, which opens gate 3 of counter 1, and the cycle again repeats; 250 millisec after the 8-millisec one-shot has been triggered, flip-flop 3 of the channel selector has its state changed by another 8-millisec one-shot. The output of this flip-flop activates gates 4 or 5 to counter 2 and also produces the same sequence of events as flip-flops 1 and 2. The 250-millisec delay allows the printer to print the information from counter 1 before starting the cycle associated with counter 2. The output of the 250-millisec one-shot also triggers a second 250-millisec one-shot, which in turn operates on channel selector flip-flop 4 and counter 3 in the same manner as was described for flip-flop 3.

It is conceivable that information may be recorded on the printer five times in rapid succession. However, owing to the frequency of the cosmic dust reset and ion chamber pulses, this is usually not the case. In most cases, the information in the three counters will be printed out in 260-millisec steps, followed by a 5-sec (or greater) delay between the ion chamber and cosmic dust information printout. It is recommended that an EPSCO logic handbook be referred to if a more complete description of this logic is desired by the reader.

9. Oscilloscope (Tektronix,[4] Model RM561)

The oscilloscope is primarily used for the examination of signals from the spacecraft experiments and the DAS. It is also a very useful tool for troubleshooting anywhere in the GSE system.

10. Oscilloscope Selector

Inputs to the oscilloscope can be selected by rotary switches on the scope panel without moving any test leads or disturbing the system. For versatility, both the high and low scope inputs are changed by the selector switch. These inputs can be easily revised by changing patches at the patchboard.

11. Analog Selector

Analog signals from the spacecraft experiments displayed on the DVM are selected by use of rotary switches. The DVM scan and print cycle is remotely controlled by a DVM read command on the analog select panel.

12. Oscillograph Recorder (Minneapolis-Honeywell,[5] Model 1508)

The 24-channel capability of the Visicorder is utilized to give a printed record of voltage steps and ac signals for comparison purposes. Since the input impedance of the galvanometers used in the Visicorder is relatively low, all signals displayed on the Visicorder are isolated with amplifiers to prevent signal loading.

13. Digital Recorder (Electro Instruments,[6] Model 9055)

This printer is used with the count rate accumulator system and records the digital outputs from the particle flux and the electron flux experiments. For ease in data reduction, the output of the cosmic dust experiment is printed in a 6-bit binary code, and GSE clock time is printed out every time an ion chamber pulse is monitored.

14. Patch Panel (Mac Panel,[7] Model 911)

All command and signal functions from and to the spacecraft and the GSE appear at the patch panel for monitoring and signal routing, thus providing greater flexibility as to functions monitored and test equipment used as well as a definite control over the grounding scheme employed.

15. Power Supply (Dressen-Barnes)

GSE Unit 20A2-9 contains two 28-v Model 21-112 power supplies used for the voltage-scanner, stepping-switch-controlled circuit relays and all indicator lights.

16. Power Supply (Correlated Data Systems[8])

This unit supplies a 52-v, peak-to-peak, 2400-cps squarewave to the spacecraft TR and to the GSE clock, and also an 18-v, peak-to-peak, 4800-cps squarewave to the spacecraft inverter. Power to the spacecraft inverter or TR is only used in a subsystem configuration when spacecraft power is not available.

C. *Miscellaneous Test Equipment*

1. Low-Energy Ion Current Injection Probe

A 10^{11} ohm resistor is mounted in a shielded chassis approximately 1 ft from the low-energy ion experiment.

[4] Tektronix, Inc., Portland, Ore.

[5] Minneapolis-Honeywell Regulator Co., Denver, Colo.

[6] Electro Instruments, Inc., San Diego, Calif.

[7] Mac Panel, High Point, N. C.

[8] Correlated Data Systems Corp., Glendale, Calif.

By varying the output of a precision voltage source at the GSE, a current with a magnitude from 1×10^{-11} to 20×10^{-11} amp is injected into the collector of the low-energy ion electrometer through a low-capacitance shielded cable. A rotary switch on the GSE control panel selects the voltage applied to the current probe resistor. For versatility in current injection, individual potentiometers regulate the output voltage for each of the five switch positions.

2. Isolation Box (Unit 20A5)

Isolation amplifiers are required for all functions from the spacecraft monitored by the GSE to prevent deterioration of spacecraft signals due to cable capacitance. Pulse-shaping amplifiers are used to condition the command signals from the GSE, since a definite pulse shape was required by most experiments for proper operation. The command source selection relays, signal conditioning amplifiers, and isolation amplifiers are mounted in an isolation box approximately 5 ft from the experiments. Figures 76 and 77 are, respectively, a photograph and a schematic diagram of the isolation box.

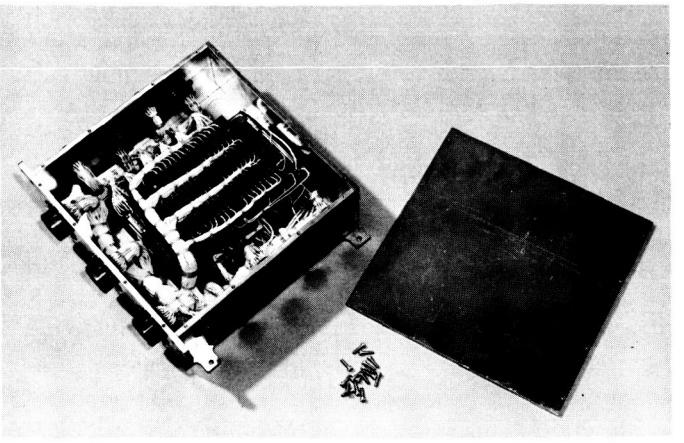


Fig. 76. Isolation box

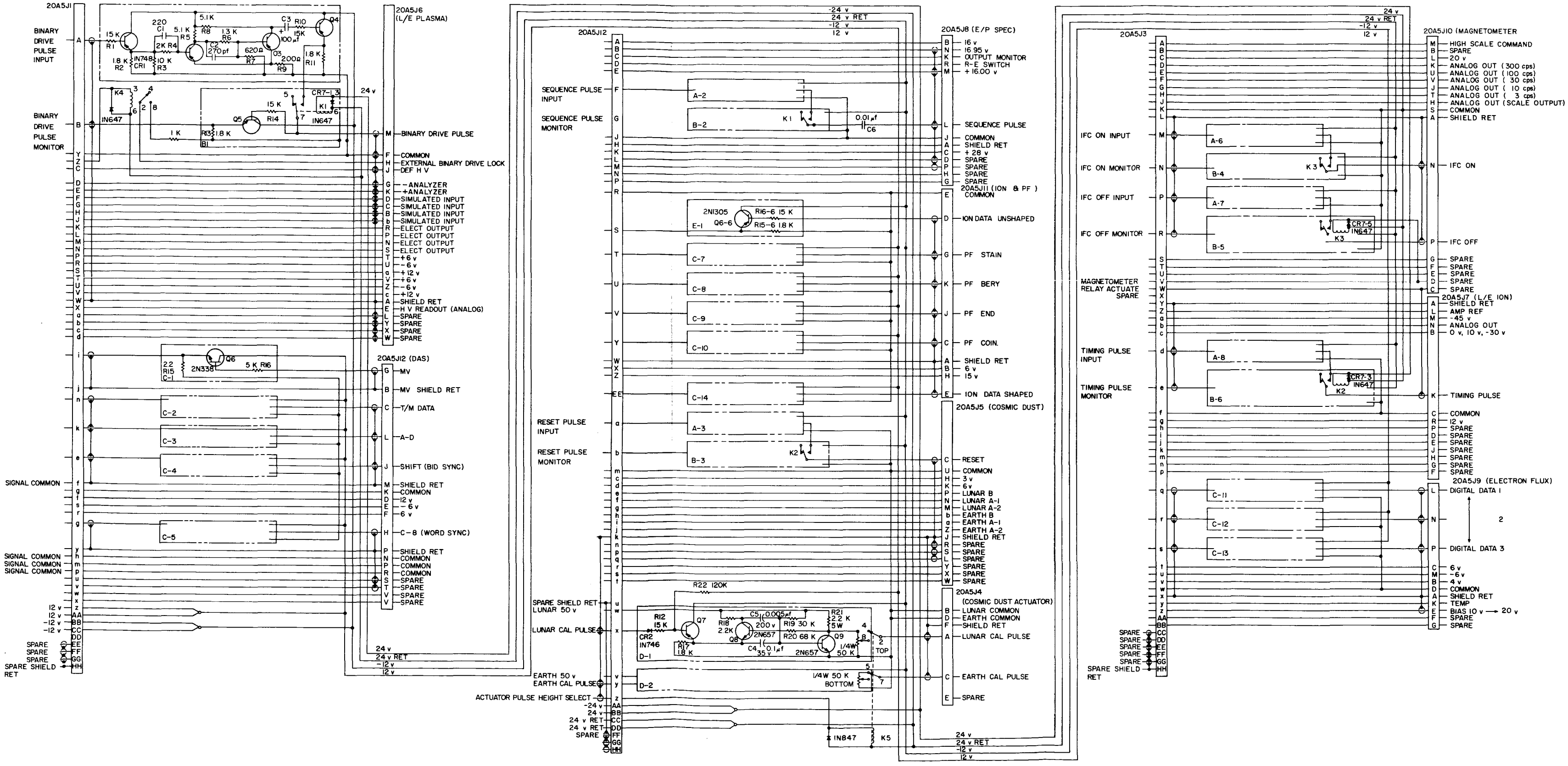


Fig. 77. Scientific isolation box

XV. DATA AUTOMATION SYSTEM GSE

The DAS GSE when operated in conjunction with the scientific GSE can completely evaluate the electrical performance of the DAS. The GSE is primarily intended to provide quick-look information for a go/no-go evaluation of the DAS, but verification of DAS information conversion is also possible by comparing the DAS coded output with the experiment's raw data output at the science GSE.

A. Test Conditions and Checkout Procedures

A brief description of the DAS test conditions and checkout procedures is as follows:

1. Preliminary Checkout

Power is provided by the GSE to the DAS transformer rectifier via the science TR unit. The science GSE generates the 400-cps sync signal which simulates the CC and S input to the DAS.

1. The particle flux selector switch on the experiment simulator control panel provides a 400-cps square-wave signal to the DAS isolation box, where it is signal-conditioned by a one-shot and sent to all four particle flux inputs of the DAS. The DAS makes a digital-to-binary conversion of this information and sends the coded word plus a bit sync signal through emitter followers in the science isolation box to the science GSE. This information is routed to the science data translator in the DAS GSE, which converts the data to an octal format for quick-look printout on paper tape and on punch tape for teletype transmission. DAS checkouts with simulated electron flux and ion chamber experiment inputs are performed in the same manner.

2. Cosmic dust simulation consists of selecting one of four 6-bit binary codes at the experiment simulator control panel and displaying it to the DAS through the DAS isolation box. The DAS converts the 0- and 6-v levels to a binary word and sends this information to the SDT for tape printout.

3. Analog signals representing the magnetometer outputs are selected at the experiment simulator control panel and sent to the DAS through the DAS isolation box. These analog voltages may be adjusted to any desired voltage by means of three potentiometers located on the experiment simulator panel. A visual indication of these voltages may also be displayed on the DAS GSE meter panel. The DAS makes an analog-to-decimal conversion of the simulated voltages and sends this information to the SDT for tape printout. The low-energy ion, electron-proton spectrometer, and low-energy plasma experiment inputs are checked out in the same way.

2. Subsystem Test

The subsystem test is a compatibility check with the experiments providing inputs to the DAS. The data obtained from the DAS GSE are compared with the data from the scientific GSE; all the readings should be the same.

B. Description of Equipment

A block diagram of the physical location of each of the components that make up the racks is shown in Fig. 69. A brief description of these components is as follows:

1. Meter Panel

Three GE panel voltmeters are used for quick-look applications, and a four-position selector switch is used to choose the meter inputs. The first, second, and third positions display the DAS dc voltages, the SDT power supply voltages, and the experiment simulator control analog voltages, respectively. The fourth position connects all three meters to the patch panel so that any voltage desired to be displayed can be conveniently patched in. Figure 78 is a schematic diagram of the meter panel.

2. Experiment Simulator Control Panel

This panel is used to simulate the experiment outputs when checking out the DAS independently. The first five switches control the application of four different analog voltages to the DAS to simulate the low-energy plasma, low-energy ion, electron-proton spectrometer, and magnetometer experiment analog voltages, and the temperature analog voltage from the low-energy plasma, electron flux detector, and particle flux experiments. The cosmic dust detector selector switch is used to simulate four different binary codes to the DAS. The different analog voltages used for simulation are derived from a simple voltage divider shown on the schematic in Fig. 79. The three potentiometers can be individually adjusted to provide different analog voltages for the first, second, and

third switch positions. The remaining two switches control the electron flux, particle flux, and ion chamber simulation to the DAS. When either switch is turned on, a 400-cps signal is sent to the appropriate DAS inputs through the DAS isolation box.

3. Digital Recorder (Hewlett-Packard,[9] Model 562)

This printer is used to record the octal word outputs from the science data translator. Real time and test step number are also recorded.

4. Tape Perforator (Tally,[10] Model 420 PR)

The output from the SDT, in TTY format, is recorded on punch paper tape by the tape perforator. This tape is filed as a permanent record of all tests.

5. Power Supplies (Dressen-Barnes)

GSE unit 20A3-8 contains two power supplies used for the following applications:

1. −6 vdc, Model 22-211. Used for the count rate accumulator.
2. +31.5 vdc, Model 22-217. Used for the spacecraft inverter unit.

GSE unit 20A3-9 contains two power supplies used for the science data translator:

1. −15 vdc, Model 25412.
2. +10 vdc, Model 22-113A.

6. Clock Relay Chassis

This unit contains 22 emitter followers and 22 relays. Input logic levels indicating real time and test step are obtained from the scientific GSE and drive the emitter followers, which in turn actuate the relays. The relay contacts are connected to the SDT and are periodically sampled. This time is printed out on the Hewlett-Packard digital recorder. Figure 80 is the clock relay schematic.

7. Science Data Translator

The science data translator (SDT), in conjunction with the Hewlett-Packard digital recorder and the Tally tape perforator, provides the means by which the binary information from the DAS is coded and printed out in octal notation. A complete description of this operation is given in Section XVI.

C. *Miscellaneous Test Equipment*

The isolation box (Unit 20A4) serves two purposes (see Fig. 81):

1. It provides a convenient junction point for the analog voltages from the experiment simulator panel to the DAS.
2. It contains signal-conditioning amplifiers for the 400-cps signal to the DAS.

[9] Hewlett-Packard Co., Palo Alto, Calif.
[10] Tally Register Corp., Seattle, Wash.

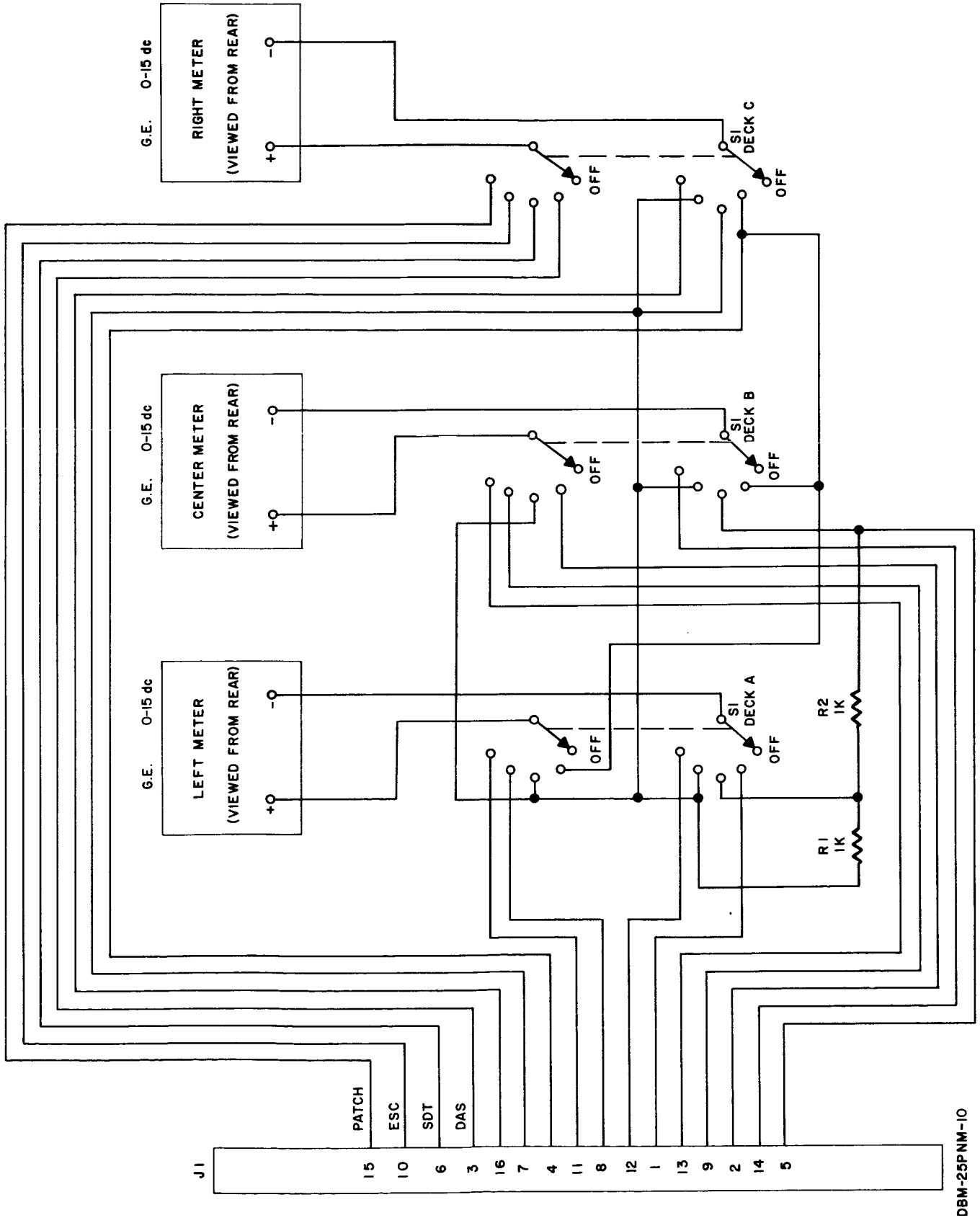


Fig. 78. Meter panel schematic diagram

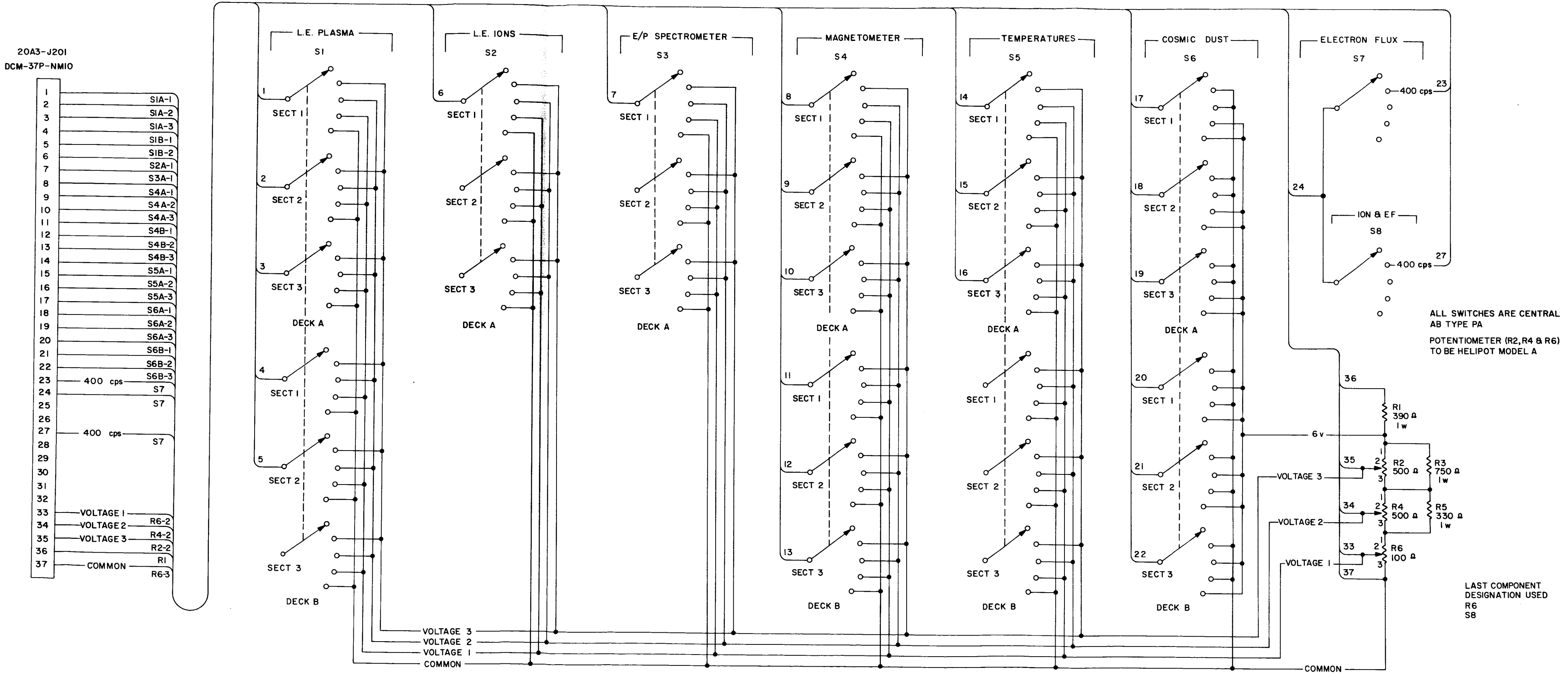


Fig. 79. Experimental simulator control panel, schematic diagram

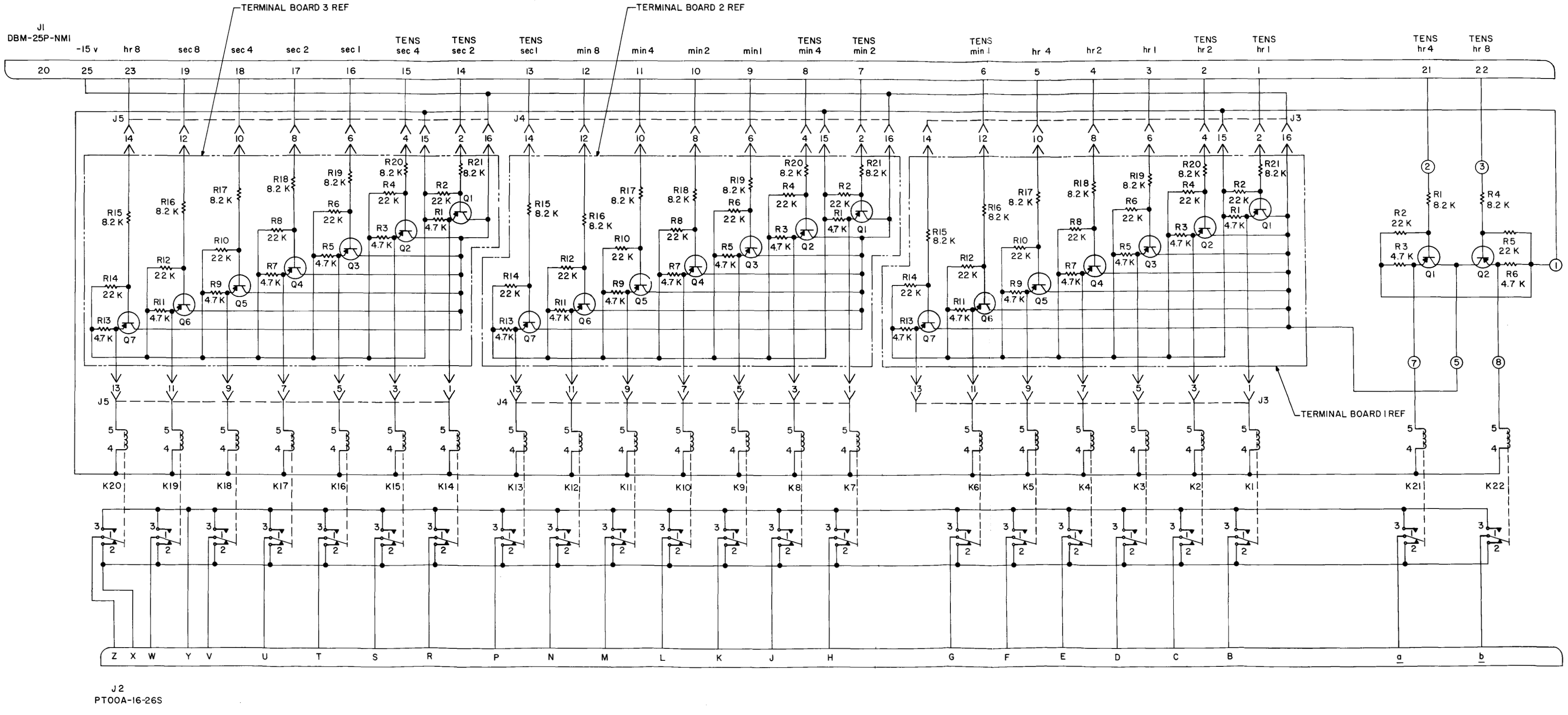


Fig. 80. Clock relay schematic diagram

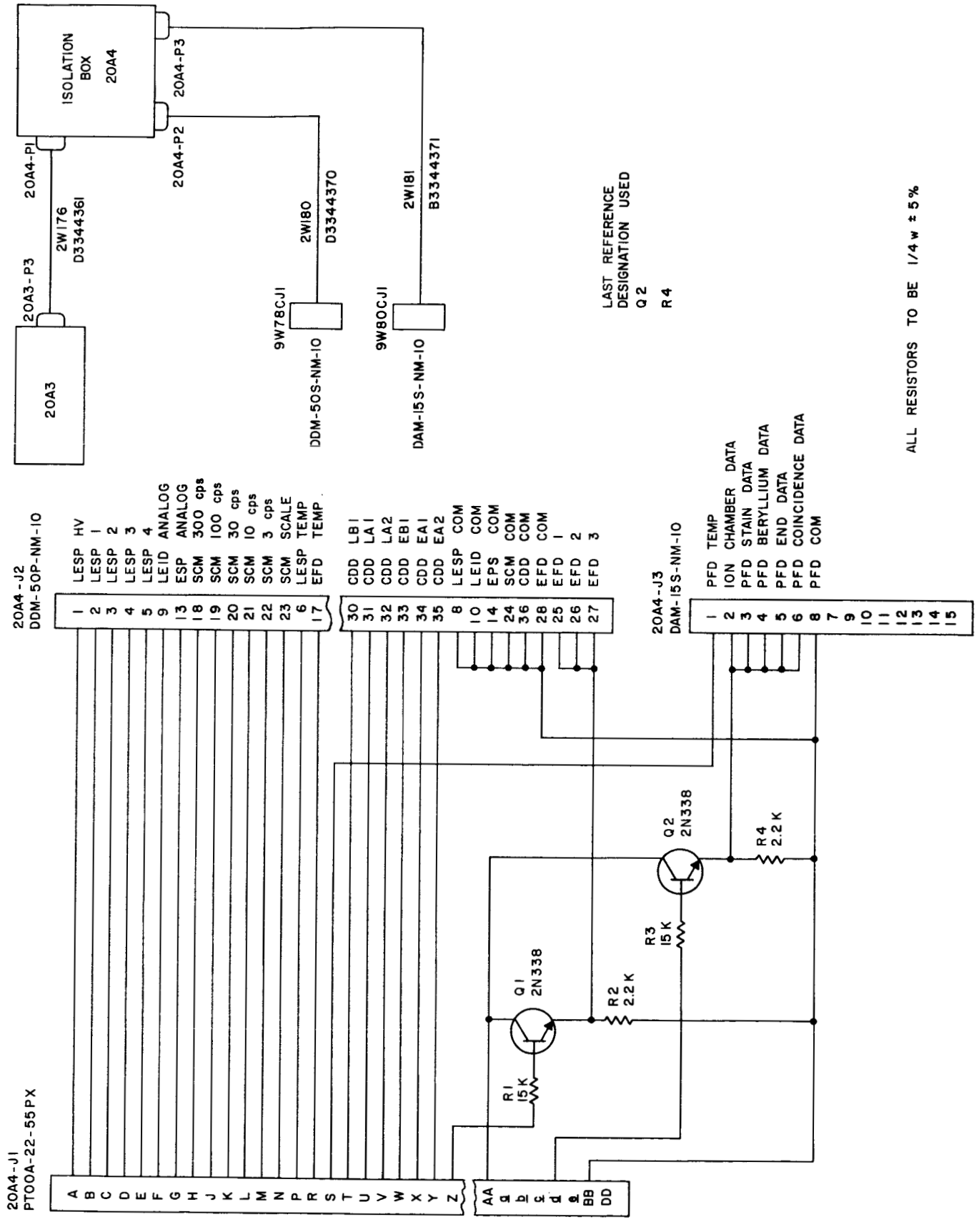


Fig. 81. DAS isolation box schematic diagram

XVI. SCIENTIFIC DATA TRANSLATOR[11]

A. Physical Description

The Scientific Data Translator (SDT) is an equipment complex designed to accept the coded signals from a spacecraft Data Automation System (DAS) and convert this information into a form compatible with the transmission characteristics of a commercial teletype circuit and/or provide *quick-look* printed output suitable for operation evaluation.

Design of this equipment, together with the format characteristics of the spacecraft DAS, is such as to make the SDT directly applicable to both the *Mariner* and *Ranger* Follow-On programs.

The SDT is suitable for use at DSIF tracking stations or as an integrated element of the ground support equipment associated with the spacecraft DAS.

The SDT consists of three physically separate elements: (1) a logic drawer, (2) two output mechanisms, a digital recorder and a paper tape punch, and (3) a power supply. If installed at a DSIF site, the output mechanism would be the paper tape punch. Under this condition, the entire equipment complement is physically interchangeable with the Telemetry Support Equipment (TSE) currently installed.

1. Logic Drawer

The logic drawer consists of a framework, provided with a front panel, suitable for mounting three DEC (Digital Equipment Corporation) type 1909 mounting panels, each capable of accepting 25 DEC logic modules or cards.

The drawer is designed for installation in a standard relay-rack type of equipment cabinet. It is provided with standard chassis track type drawer slides having tilt mounts, permitting access to the equipment from the front of the equipment cabinet for maintenance.

Front panel dimensions of the logic drawer are 19 in. wide by 8¾ in. high, both standard for the application and identical to the *Ranger 1* and *2* TSE, to facilitate interchanging the panels.

[11] This section was previously published by JPL as Section Report No. 324-5.

Mounted on the front panel of the SDT are the status display and all controls necessary for operation/maintenance of the equipment (Fig. 82).

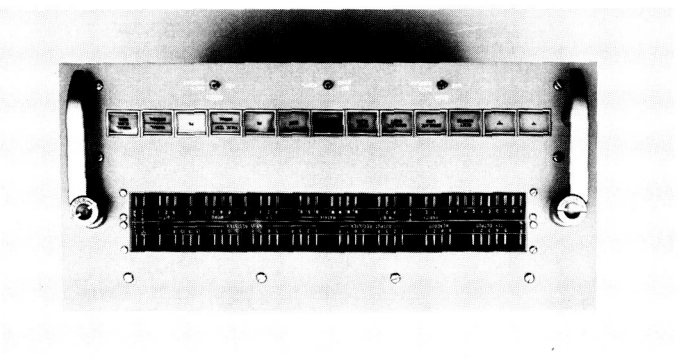


Fig. 82. SDT front panel layout

Connections to the logic drawer are made through several multicircuit connectors at the rear of the logic drawer.

2. Output Mechanism

Associated with the logic drawer is a mechanism capable of converting the electrical signals from the SDT logic into either teletype (TTY) format punched paper tape for subsequent transmission, or printed data for visual inspection, or both.

a. Digital printer. Preparation of printed hard copy is accomplished by a Hewlett-Packard model 562 digital recorder. The 562 digital recorder is a transistorized electromechanical device providing a printed record of electronic digital information. The input to the 562 is parallel-entry four-line BCD code (1248). Up to eleven decimal digits may be printed on each line.

b. Perforator. For applications of the SDT where no hard copy requirements exist, typically at DSIF tracking sites, the output mechanism will be a Tally Register Corporation model 420 tape perforator equipped with an integral model 1424 transistorized perforator drive package.

This mechanism is completely self-contained and self-powered from the utility mains. The equipment is used as supplied, without modification.

3. Power Supply

Power for the logic drawer is derived from three Dressen–Barnes transistor power supplies and a 1-v filament transformer for the 6977 display indicator tubes.

B. Functional Description

The SDT is a data-processing mechanism inserted in the information link between the output of the spacecraft DAS and an observer. For those applications where the observer is at the location of the SDT, it provides output in the form of directly readable hard copy. For use at points remote from the observer, the SDT produces, as its output, a punched paper tape in TTY format which, when transmitted over commercial TTY circuits, provides a hard copy identical to that generated for the local observer situation.

Input to the SDT may be obtained directly from the DAS for bench check-out applications, or from the telemetry decoder for system test or actual flight applications.

To perform its functions, the SDT is provided, internally, with two basic divisions: (1) a serial data shift register and (2) an appropriate timing system. Several additional functional entities are incorporated for discrete operations associated with the data.

Referring to Fig. 83, SDT functional block diagram, the serial data shift register occupies the upper area of the figure, while the timing system is in the lower area. Data flow is shown in solid lines with timing and/or control flow shown dotted. Those additional functions of the SDT not directly identifiable with either of the two divisions are also obvious. The small-circle symbols appearing in this figure represent elements of the status display with the number of elements employed for each purpose shown by the figure within the symbol.

All functions shown in Fig. 83, with the exception of the TTY format converter and the TTY output, are accomplished by an appropriately interconnected complement of a variety of types of DEC logic cards. Since the mechanization of the octal-BCD/TTY conversion using DEC logic cards would result in the use of a number of different card types, the required gating structures have been assembled on a blank module type 1955. The converter card has been designated as type 1955-5. The TTY output function is mechanized by a set of six solenoids incorporated within the perforator. The solenoids are operated by signals from the logic cards. This scheme is employed to permit circuit isolation and to resolve the functional disparities between the operating characteristics of the DEC logic elements and those of the output mechanisms.

Diagrams of the SDT are a combination of three functions: (1) logic, (2) schematic, and (3) wiring. It is necessary that the logic conventions be understood at this point in order to read these diagrams in conjunction with the detail functional descriptions. DEC symbology is listed in Fig. 84.

1. Data Channel

As shown in Fig. 83, the two-level data pass serially through a *no data test* function, a 16-bit input register, and an 8-bit output register.

Data contained in the input register are tested for parity and the presence of the PN sync word.

From the input register, the data shift serially through the output register. The eight stages of this register are sampled in various set configurations at appropriate times, in accordance with the states of the control counter, or clock, and passed in parallel to (1) the TTY format converter, thence to the TTY output circuitry and associated relays, and (2) the digital recorder output circuitry.

Condition of each logical element in this data path is constantly displayed by a set of 35 individual indicators assembled into a data status display, the upper set of Fig. 82. While much of the information cannot be directly assessed quantitatively, the general character of the data register operation can be observed at full system rates. Certain indications are always significant, and all indications become significantly interpretable under slower speed test operation.

a. Data input. One output signal is provided to the SDT. This *data* signal has an assertion level of 6 v. This level is routed through a DEC-type 4504 logic card which converts the 6-v assertion level to the required DEC −3-v assertion level.

The *data* signal is also routed through an inverter, a DEC-type 4106 logic card, to generate $\overline{data}$, since this term is also required for proper operation of the SDT.

Figure 85, SDT data input logic, shows the routing of the *data* and $\overline{data}$ signals. With the four serial switches in the *operate* condition, as shown in the figure, each signal is passed directly to one negative level *and* gate, and

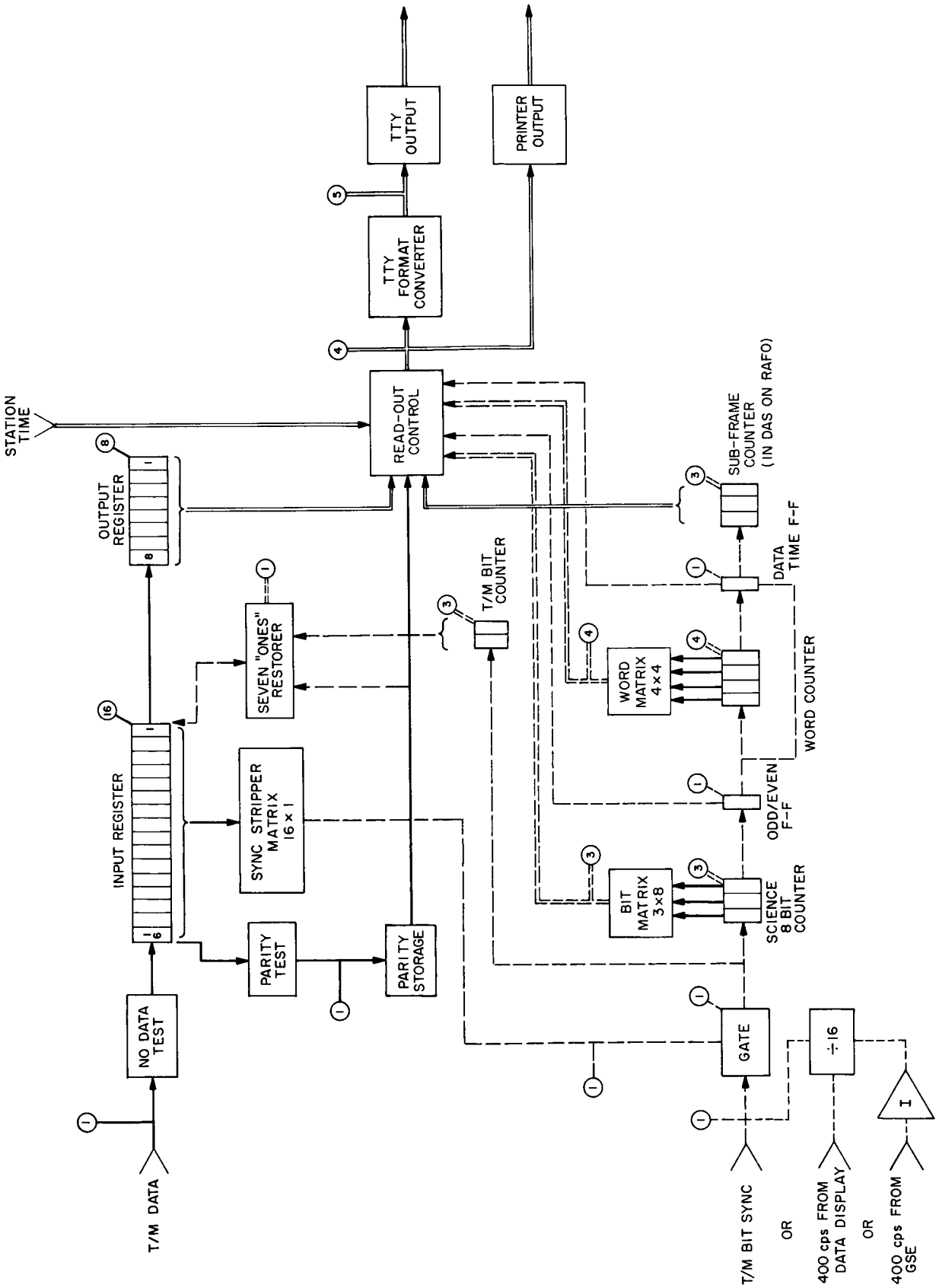


Fig. 83. SDT functional block diagram

through an inverter to the opposite negative level *and* gate. In this fashion, one *and* gate or the other is always supplied with two negative signals in the presence of input data. Since the configuration of the DEC-type 4113 logic card used in this *and* application includes an inverter following the two-input *and* gate, the output of the gate whose input requirement of two negative signals is satisfied will be an assertion signal but inverted in polarity; that is, 0.0 v. Output of the opposite gate will be a negation signal, also inverted; hence, −3.0 v, which is the clamp level of the DEC logic cards.

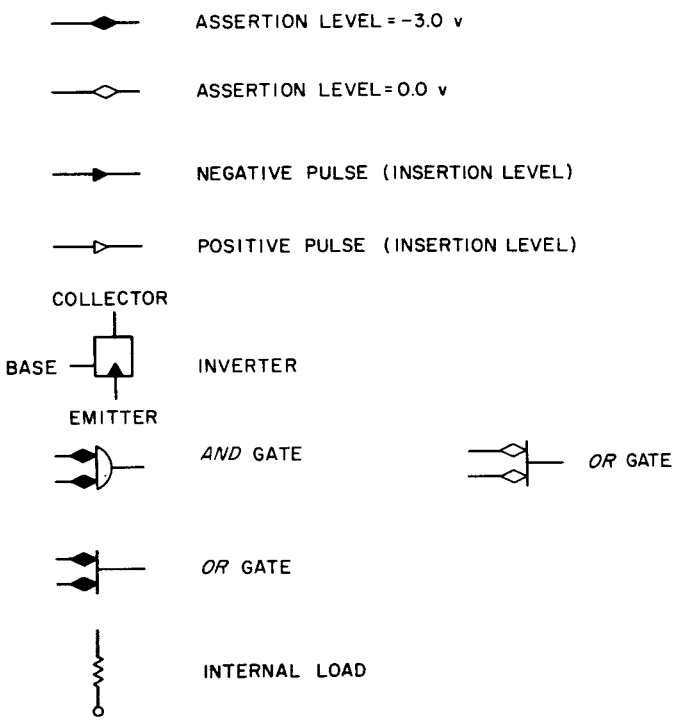


Fig. 84. Digital equipment corporation symbology

Since a level of 0.0 v is required at the input of the DEC-type 4213 shift register card to set the input, or "D" flip-flop (F-F), the lower gate will control the register input when incoming data are in the *one* state. Conversely, the upper gate will control the register input when data are in the *zero* state.

No data *test*.[12] As described above, in the presence of data from the T/M decoder, either the *data* or the $\overline{data}$ line will be negative, in accordance with whether the data are *one* or *zero*, respectively. Conversely, the line which is not negative will be at 0.0 v. Note, however, that at no time will both lines be at 0.0 v except in the absence of an input signal to the SDT.

[12] Since $\overline{data}$ are generated internal to the SDT, the *no data* test function is unable to distinguish "*no data*."

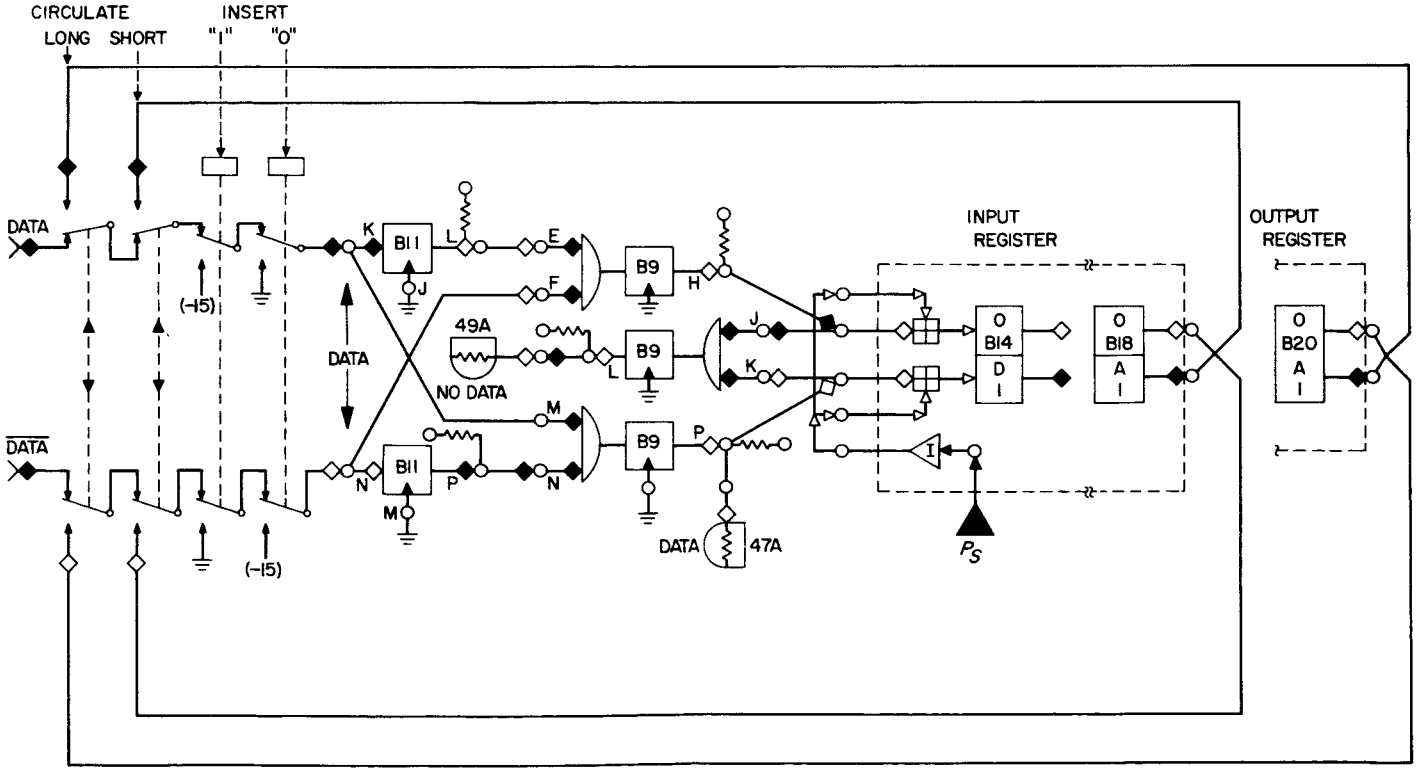


Fig. 85. SDT data input logic

When the condition of both lines at 0.0 v exists, it is obvious that the input requirement of the negative input *and* gate is not satisfied in either case; hence, both gate outputs will be negative. This condition does not constitute information input to the data input register, but the two negative signals do satisfy the input requirements of the *and* gate connected to the register inputs. Since, normally, one of the two inputs to this gate is 0.0 v, its output will be negative; but with both inputs negative, the gate output will go to 0.0 v and the associated *no data* indicator will light.

Data test capability. The maintenance philosophy for the SDT requires that it be self-sufficient for test purposes. To this end, the data input circuit is routed through a series of four test switches, all being double pole to accommodate both the *data* and $\overline{data}$ lines.

Two toggle switches are provided to permit circulating the data within the SDT registers. The first of these connects the data input to the output of the output register, resulting in a 24-bit register length. It is identified as *circulate-long*. The second switch connects the data input to the output of the input register, resulting in a 16-bit register length, and is identified as *circulate-short*.

Two momentary contact switches are provided to permit loading any desired data pattern into the SDT. The first of these applies negative voltage to the *data* line and 0.0 v to the $\overline{data}$ line, corresponding to a data *one*. The other applies 0.0 v to the *data* line and negative voltage to the $\overline{data}$ line, corresponding to a data *zero*. These switches are appropriately identified as *insert 1* and *insert 0*, respectively.

Note that the position and contact arrangement of the *insert* switches is such as to make them operate regardless of the settings of the *circulate* switches; furthermore, they may be operated with the SDT connected to the T/M decoder and in normal operation without compromising the decoder output.

2. Data Registers

Input and output data registers, with their associated functions, are shown in their entirety in Fig. 86.

The total of 24 bits represented by the combined capacity of these two serial registers is stored in six DEC-type 4213 logic cards, containing four F-Fs each. The diagram groups the F-Fs in sets of four, similarly to the physical arrangement. Likewise, the grouping of the individual indicators in the status display, Fig. 82, follows the hardware configuration.

Attention is directed to a situation which appears to be an inconsistency but which, once recognized, facilitates use of both the display and the diagrams. The display presents the most significant bit (MSB) in the left position, the normal reading position such as that of the accumulator register of a desk calculator. Shifting data thus progress from right to left, least significant bit (LSB) to MSB, in the status display. In the logic/schematic diagram, Fig. 86, however, signal flow follows the normal practice of progressing from left to right, thus reversing the positions of the MSB and LSB from those of the status display.

Input to the input register is shown on the left side of Fig. 86, as it is derived from the data input logic, Fig. 83. The assertion and negation levels shown symbolically at the register input, as well as throughout the register, correspond to a data *one*. Certain properties of the type 4213 shift register logic cards must be recognized in conjunction with the presence of both the assertion and negation signals at the input to each of the 24 F-Fs. Since the input to the F-F is through a capacitor-diode gate, in which a DEC standard positive pulse is *and*ed with the input signal, the signal required to produce an input to the F-F itself must be non-negative, or 0.0 v. In order to shift either *one*'s or *zero*'s through the register, it is necessary to have an input to either side of the F-F, in accordance with the state of the preceding stage. Cross-connection from the *one* output of one F-F to the *zero* input of the following F-F is required because, since the output is unbuffered, the signal level is inverted by passage through the F-F. Thus, whereas a 0.0-v level is required at the input to the capacitor-diode gate on the *one* side of a F-F in order to set the F-F to the *one* state, the output from the *one* side of the F-F, after it is set to the *one* state, will be a −3.0-v level. Conversely, the output from the *zero* side of a F-F, which is in the *one* state, will be 0.0 v—hence, the cross-connection.

As a result of the properties described above, the requirement exists for *both* input gates of the shift register F-Fs to be connected to input information. Because of the input gate configuration, an input left floating acts as if a level of 0.0 v existed on that input. Thus, if a true signal level of 0.0 v exists on one input gate and the other is unconnected, the total input is ambiguous and the probable state of the F-F, following a shift pulse, is completely indeterminate. Similarly, presence of a −3.0-v level on both input gates simultaneously will result in no

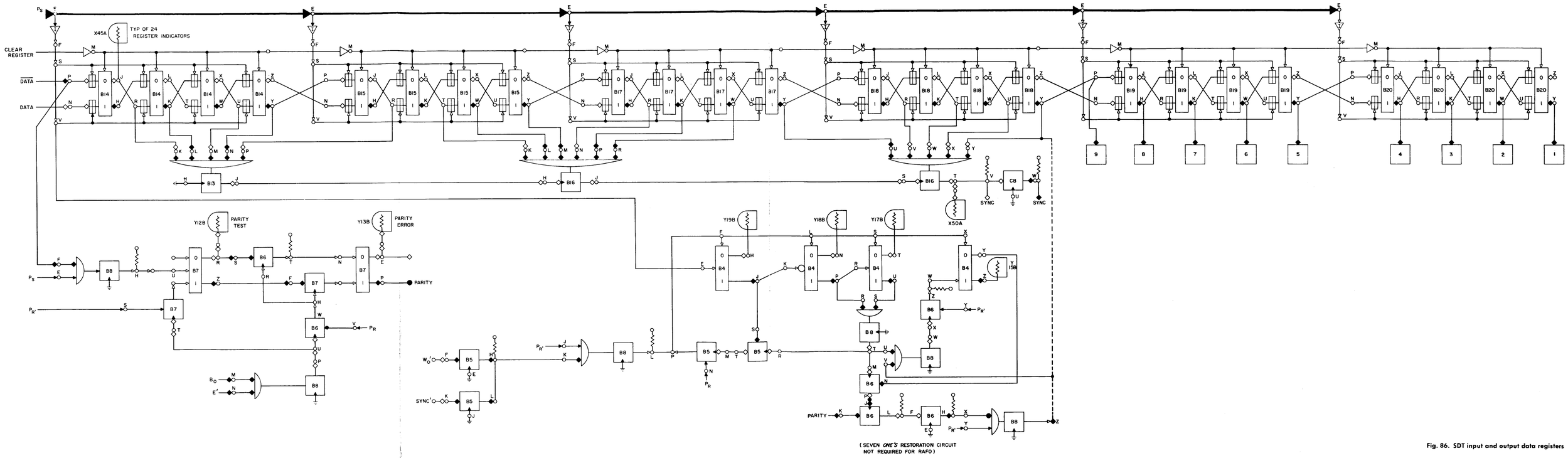


Fig. 86. SDT input and output data registers

input to the F-F, which will retain its state regardless of the occurrence of a shift pulse.

Type 4213 cards incorporate an inverter capable of driving all gates simultaneously, so that the required shift pulse to the card is a DEC standard negative pulse, which results in the DEC standard positive pulse necessary for operation of the input gates. A *reset* input, affecting all four F-Fs on *one* card, is also provided. This latter capability is used to clear, simultaneously, all 24 stages of the combined input/output registers.

Sync stripper. The data shifting through the 16-bit input register are under constant surveillance by the 16 × 1 sync stripper matrix in order that presence of a sync word will be detected. The sync word is a 15-bit reentrant pseudonoise sequence, followed by a parity bit to fill out the normal 16-bit word. Reading from left to right, with the MSB at the left, in accordance with its appearance in the status display, the sync word is as follows:

0000 1110 1100 1010

F-F states corresponding to the presence of this sync word in the input register are given in Fig. 5, above the individual F-F symbols.

One or *zero* outputs, appropriately, from each of the 16 F-F's are combined in the sync stripper matrix, consisting of three type 4111 six-input negative *and* gates. Connecting the three inverters of the *and* gates in series effectively creates one 18-input *and* gate. Two of these inputs are unused; however, in the case of the type 4111 diode-register *and* gate they may be left floating without disturbing operation.

Output of the sync stripper 16 × 1 matrix, because of the presence of the inverters following the negative *and* gates, is a level of 0.0 v at the top of the three inverter string. This state will persist as long as the PN sync word stands in the register. The 0.0-v state is compatible with the *turn-on* requirements of the type 6977 indicator tubes and is used directly to light the sync indicator, No. 50A, in the status display. An inverter follows the 0.0-v assertion output of the three type 4111 *and* gates to produce a −3.0-v level assertion output required for *down-logic* application.

Output of the sync stripper is used to synchronize the SDT logic with that of the spacecraft DAS.

Parity test. The data transmitted from the spacecraft DAS are formated into groups of 15 data bits followed by a parity bit. The parity criterion is that the 16-bit group must contain an *odd* number of *one*'s. Thus, the 15-bit data group consisting of all *zero*'s will be followed by a *one* in the parity bit position.

Parity verification is accomplished in the following manner, with the explanation predicated upon the assumption that the sync word is standing in the input register, as a starting point. Validity of this stipulation is based upon the fact that the sync stripper performs its own parity check by testing all 16 bits of the sync word which includes the parity bit, together with the 15 bits of the sync word PN sequence.

Proceeding with the explanation: the situation in which any complete 16-bit group, sync word or otherwise, occupies the input register is defined by the SDT clock in terms of the states of an *odd/even* F-F and an octal bit counter. The particular clock time of concern here is identified as $E'B_0$.

Reference to Fig. 86 will show that E' and B_0, both in *down-logic*, are applied to the input of a two-input negative *and* gate, DEC-type 4113, whose inverter produces a 0.0-v level at time $E'B_0$. The level is *and*ed, through DEC-type 4106 inverters with two timing pulses, P_R (pulse-read) and P'_R (pulse-end of read interval).

The signal $P'_R E'B_0$ is used to set the parity test F-F to its *one* state, in which condition its *zero* output is at 0.0 v, turning on the *parity test* indicator 12B in the status display.

The input to the *zero* side of the LSB flip-flop (bit position 16) of the input register is combined, through a two-input negative *and* gate, with P_S (shift pulse). Thus, a positive-going pulse will appear at the output of the inverter of the *and* gate immediately preceding each shift operation which reads a *one* into the LSB position of the input register.

This positive-going pulse is the signal necessary to complement the parity test F-F. Since the F-F was stipulated as being in the *one* state immediately prior to shifting the MSB of the following word into the input register, it is obvious that it will be in the *zero* state whenever an *odd* number of *ones* has been shifted into the register. When a total of 16 bits has been shifted into the input register, the timing cycle will have been completed and the $E'B_0$ condition will exist again.

At this time, the state of the parity test F-F indicates whether or not the parity requirement has been satisfied for the 16-bit group standing in the input register, and this information is transferred to the parity error storage F-F.

This function is accomplished by *and*ing the $E'B_0$ condition with the P_R pulse in a type 4106 inverter. The $P_RE'B_0$ signal is *and*ed with either the *one* or the *zero*, whichever one is in the −3.0-v state, the output of the parity test F-F to serve as a positive-going pulse to either the set *one* or set *zero* input of the storage F-F.

As in the case of the parity test F-F, the *one* state of the storage F-F corresponds to a parity error, and accordingly, the *parity error* indicator 13B in the status display is connected to the *zero* output of the storage F-F, which will be at 0.0 v for a parity error condition.

Immediately following the transfer of the parity information to the storage F-F, at P_R time, the parity test F-F is again set to the *one* state, at P'_R time, as described at the start of this explanation.

The parity storage F-F thus holds the parity information for a particular 16-bit group for the entire time that this group is being shifted through the output register.

Seven one's *restoration*[13]. During part of the *Mariner* mission, science data and engineering data are transmitted alternately over the same T/M circuit. The sync information required by the T/M decommutator is a pattern of seven consecutive *one*'s, which will never exist in the engineering data. Unfortunately, this pattern could occur as meaningful information in the science data and, since the decommutator is not arranged to recognize the fact that the transmission containing the seven *one*'s is scientific data, considerable confusion might result.

To protect this characteristic of the T/M decommutator, the spacecraft Data Conditioning System (DCS) has been so set up that, should its output include a series of seven consecutive *one*'s lying wholly within a 7-bit T/M word, the last (7th) *one* will be complemented to a *zero*. This change takes place *after* the DCS has generated the parity bit for the 16-bit group containing the complemented bit; thus, the lack of parity is the significant piece of information upon which the restoration process, within the SDT, is based.

[13] This circuit is not required for *Ranger* follow-on. It has been disabled by removing the output wire from B8-Z to B18-Y.

Two basic elements comprise the seven *one* restoration function: (1) the T/M 7-bit/word counter and (2) the data processor (Fig. 86).

The counter consists of three of the four F-Fs comprising a DEC-type 4215 logic card. These are arranged to count, in binary progression, from zero through seven inclusive. The counter is reset to zero each time the count of seven is reached by a three-input *and* gate consisting of a two-input gate, type 4113, connected to the 2_2 and 4_2 F-Fs and an inverter type 4106 connected to the 1_2 F-F. The output of this inverter and P_R are applied to another inverter *and* gate to produce the required positive reset pulse.

Synchronizing of the T/M 7-bit/word counter is based upon the fact that the first bit of the DCS sync word is also the first bit of a T/M word. Thus, when the sync stripper output comes true at word zero (W_0) time, the read pulse $(P_R)'$ is fed to counter reset inputs, ensuring that this counter starts in synchronism with the basic SDT clock, which is, by definition, in synchronism with the 7-bit T/M words.

Use of the $(P_R)'$ pulse to synchronize this counter is based upon the requirement of the 4215 logic card that input and reset signals not exist at the same time if ambiguity is to be avoided. Since $(P_R)'$ occurs significantly after P_S, the requirement is satisfied. Similarly, inclusion of the W_0 term in the *"sync reset"* expression is to preclude resetting this counter when the PN sync word occurs as the master frame identifier.

Data processing for the seven *one's* restoration is based upon the premise that occurrence of a *zero* in any of the first 6-bit positions of the 7-bit word is equivalent to *not* having six *one*'s in these positions. This premise is mechanized in the following manner:

The output of the two-input negative *and* gate connected to the 2_2 and 4_2 F-Fs will be negative for counter states *zero* through five. This negative level is used as one input to a second two-input *and* gate, the other input being the output of the zero side of the MSB position of the input register. The input requirements of this gate will be met if a *zero* is shifted into the MSB position during the time the T/M counter advances from the *zero* state through state five, corresponding to the first 6 bits of a T/M word. If this occurs, the gate output is used with P'_R in an inverter *and* operation to produce a positive pulse which sets a F-F to the *one* state, indicating that restoration of a *one* is not required. If a *zero*

is not detected in any of the first 6 bits, the flip-flop remains in the *zero* state, and when the T/M counter reaches state 6, corresponding to the 7th bit of a T/M word, the output of the state 6 detector and the *zero* output of the F-F are used as inputs to an inverter *and* gate.

This gate output is used as the emitter input of another inverter *and* gate, the other input being the parity signal. If a parity error exists for the word in the register, there will be a positive output from this gate, which is then inverted and used as one input to a type 4113 *and* gate, the other input being P'_R.

The output of this gate, which will be at 0.0 v if the input requirements are satisfied, is tied directly to the *zero* output of the unbuffered F-F, in the type 4213 register card, at the MSB position of the input register. Since this point will be at −3.0 v if the register holds a *zero* in this position, forcing the point to 0.0 v will change the register F-F to the *one* state, completing the required complementing operation.

Condition of the restoration F-F is indicated by the 7 × 1, 15B light in the status display. Since this indicator is connected to the *one* output of the F-F and requires 0 v to light, it will come on and remain on until a *zero* is detected. If the indicator is on when entering state 6 of the T/M counter, the complementing action should be observed in the MSB position indicator 27A of the input register in the status display. Conversely, should the complement requirement not exist, the 7 × 1 indicator should go off prior to counter state 6.

Output register. The output register is an extension of the input register, having all the common properties described previously.

In connection with Fig. 86, the only significant item relating to the output register is the use of the square enclosing the bit position number of the *one* state wire terminating at the square. This same delineation will be used in conjunction with the read-out control logic yet to be described.

2. Timing

The function of the SDT, as previously described, is to accept the serial binary representation of data which has been fed to the spacecraft DAS and present this information in a different and more useable form and arrangement. In this case, one of the operations performed is the collection of binary bits into octal digits, following which the octal digits are grouped into words in accordance with the output format of the DAS. These words are then further grouped into partially cyclic sets, or subframes, and the subframes into frames.

To facilitate observer interpretation of the above arrangement of the information being fed to the SDT, a prescribed logical appearance is given to the printed record resulting from the SDT operation. In addition, the time of receipt of the information is included in the SDT output, together with notation relative to parity errors in the incoming data and a subframe count.

An arrangement of information such as described above is referred to as "format" and is the result of adherence to a prescribed operation program in correct time relationship with the incoming data, which must have their own arrangement, or format, also. Thus, the SDT is, in reality, a data processor of the type known as a format-to-format converter.

a. Output format. The electrical output of the SDT appears as an arrangement of *one*'s and *zero*'s in parallel on five separate lines, together with the *start* signal on a sixth line. The *one/zero* combinations define the applicable alpha-numeric characters in standard teletype code. They are used to prepare a punched paper tape for a typewritten record (hard copy), which may then be read through a tape reader for TTY transmission.

The SDT output to the digital recorder appears as an arrangement of *one*'s *and zero*'s in parallel, on eight separate lines, together with a ninth line for parity error notation, a tenth line for the *print* signal, and two other lines for "0" and "1" reference levels required by the recorder.

The least significant three lines of data are decoded by the digital recorder electronics as one octal character. The next three lines are handled in the same manner, as are the two most significant lines.

TTY format analysis. Appearance of the hard copy from the punched paper tape is as shown in Fig. 87. The preamble is made up prior to a data run, and its contents are a procedural matter. However, since SDT output includes only time in hours, minutes, and seconds, the preamble should include the day, station identification, and identification of the spacecraft from which the data to follow were received. The data tape is thus completely unambiguous, regardless of any subsequent marking and/or filing system. Supplemental information, such as

SCIENCE DATA FOLLOWS — MARINER R/STATION 2/DECEMBER 13, 1961

[a]22 59 02
[d] [c]
[b]377#177 377#177 377#177 377#177 377#177
377#177 377#177 377#177 377#177 377

22 59 39
377 177 377 177 377 177 377 177 377 177
377 177 377 177 377 177 377 177 377

22 59 59
377 177 377 177 377 177 377 177 377 177
377 177 377 177 377 177 377 177 377

23 00 19
377 177 377 177 377 177 377 177 377 177
377 177 377 177 377 177 377 177 377

23 00 39
3 4 5 6 7 8 9 10 11 12
377 177 377 177 377 177 377 177 377 177 } DAS DATA WORD NUMBER
13 14 15 16 17 18 19 20 21
377 177 377 177 377 177 377 177 377

23 00 59
377 177 377 177 377 177 377 177 377 177
377 177 377 177 377 177 377 177 377

23 01 19
377 177 377 177 377 177 377 177 377 177
377 177 377 177 377 177 377 177 377

23 01 39
377 177 377 177 377 177 377 177 377 177
377 177 377 177 377 177 377 177 377

23 01 59
377 177 377 177 377 177 377 177 377 177
377 177 377 177 377 177 377 177 377

LEGEND

PREAMBLE — PUNCHED ON DATA TAPE TO INSURE PERMANENT IDENTIFICATION WITHOUT RECOURSE TO POST FACTO PENCIL MARKING OR SIMILAR HAPHAZARD AND AMBIGUOUS PROCEDURES.

[a]STATION TIME — HOURS, MINUTES, AND SECONDS. IDENTIFIES TIME OF RECEIPT OF FOLLOWING DATA FRAME.

[b]FIRST SIGNIFICANT DATA WORD IN A DAS FRAME. SINCE WORDS 1 AND 2 CONTAIN PN SYNC SEQUENCE, THIS IS DAS WORD 3. THE 377_8 NUMBER REPRESENTS THE MAXIMUM COUNT, OR *ALL ONES*, CONDITION IN THIS 8-BIT WORD.

[c]SECOND SIGNIFICANT DATA WORD IN DAS FRAME, ACTUALLY, DAS WORD 4. SINCE THE WORDS ARE PAIRED IN A 16-BIT SEQUENCE BY THE DAS, AND THE 16TH BIT IS A PARITY BIT FOR THE ENTIRE SEQUENCE, THIS WORD IS ONLY 7 BITS LONG AND 177_8 REPRESENTS THE MAXIMUM INFORMATION POSSIBLE, THE *ALL ONES* CONDITION.

[d]PARITY ERROR SYMBOL APPLICABLE, INDETERMINATELY, TO ONE OR THE OTHER, OR BOTH, OF THE WORDS BETWEEN WHICH IT IS LOCATED. A TOTAL OF NINE POSSIBILITIES EXISTS FOR THE OCCURRENCE OF THIS SYMBOL — ALL ARE INDICATED IN THIS FRAME.

Fig. 87. SDT annotated format

pass number, etc., is optional, its inclusion being a simple matter of typing in the appropriate data.

Following the preamble, on the next line, are six decimal digits of time, spaced in pairs, for hours, minutes, and seconds.

The next two lines contain 19 octal digit triplets, corresponding to data words 3 through 21 of the DAS serial format. These 19 words are arranged in two lines, 10 on the upper, or first line, and 9 on the lower, or second line.

Basically, the octal triplets are grouped in pairs, with a single space between the two triplets of one pair and a double space between pairs.

The first set of data in Fig. 87, at time 22 59 02, has the # symbol inserted in the single space between each of the two triplet numbers of a pair. This symbol is used to indicate existence of a parity error within the 16-bit transmission group containing the two octal triplets. The positions of the nine parity error symbols in these two lines represent all possible positions in which a parity error indication may appear in the SDT output format.

Since the transmission format includes 15 data bits and a parity bit in each 16-bit group, and the 15 data bits comprise two data words, the allocation of word content is uneven, with the first word of a group containing 8 bits and the second word 7 bits. The 377 177 notation appearing in most of the read-out position thus represents the largest possible octal number for the 8-bit first word and 7-bit second word of each 16-bit transmitted group.

The two lines, 19 triplets or words, correspond to one transmitted data subframe of 21 words. In transmission, however, the first two words of each subframe contain a PN sequence used to synchronize the SDT with the DAS. Since this information is insignificant, it is not presented by the SDT; rather, during the time when it is available for read-out, the SDT is reading out the time information from the station clock. Thus, the first entry in the data output of the SDT is transmitted word 3, the first significant data information. The first, left pair of octal triplets on the first, upper line of data then becomes transmitted words 3 and 4, the second pair words 5 and 6, etc.

Digital recorder format analysis. Appearance of the hard copy from the digital recorder is shown in Fig. 88. Station time appears preceding each subframe of data. This is printed at the same time the unit digit of seconds is punched on the TTY tape. The octal print-out of the nineteen significant data words follows one word per line. The first word corresponds to data word 3 of the DAS serial format.

The minus sign is used to indicate existence of a parity error within the 16-bit transmission group containing the octal triplet which appears on the same line with the minus sign and the octal triplet directly below it.

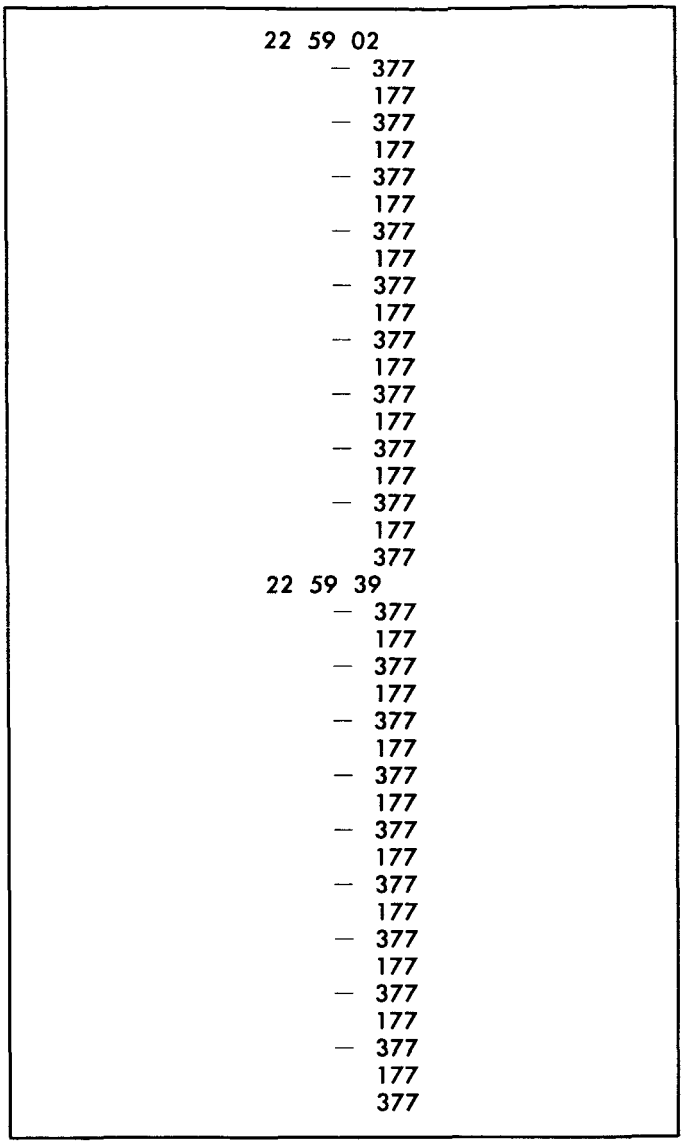


Fig. 88. Hard copy from digital recorder

Table 6 is used to convert the octal word data to analog voltages. This is done during system test to correlate the data between the DAS GSE and scientific GSE.

b. Clock. The ability to generate the output format described in paragraph B-1 above clearly requires the ability, within the SDT, to identify each of the 168 bits transmitted by the DAS as a data subframe, and further to keep track of the relationship between subframes and master frames. Furthermore, the method of bit identification used must be derived from the synchronizing information contained in words 1 and 2 of each subframe while simultaneously being compatible with operational requirements of the output format.

The major differentiations required consist in identifying the first two words of a subframe and the points in time where particular read-out or TTY control functions are necessary.

Arrangement of the SDT clock is shown in Fig. 89. It is seen to contain a counter to identify the 8 individual bits of each half of the 16-bit transmitted group, an "E" F-F to identify the *odd/even* significance of the transmitted 8-bit set within the 16-bit group, a counter to keep track of the 16-bit groups, or words, and an "F" F-F for the purpose of separating the first 16-bit group, or word, from all the remaining words. Following this is the 6-state subframe counter.

Application of the various pieces of counting information is shown in the timing table, Fig. 90. Several points are immediately obvious from this table. The carriage return, line feed, and figures shift operations occur in word zero. (W_0), regardless of the state of the "F" F-F; the same statement may be made relative to their occurrence in W_5, since W_5 exists only when F is true. Similarly, the time read-out occurs when F is false, without regard for word count, since F is false only during W_0.

With the exception of the data read-out at B_5, B_6, and B_7 in W_9, together with the machine functions previously noted, all other operations are the same for all words, from W_0 through W_9 inclusive, when F is true.

Two sets of numbers are shown for each data read-out. Those in rectangular boxes correspond to the *one* output of the output register F-F's, which are correspondingly marked. The unenclosed numbers are the binary bit identifications within each data word which are read out as octal digits from the corresponding register positions.

Referring again to the diagram of the clock, Fig. 89, the elements corresponding to the requirements of the timing table, Fig. 90, are readily identified. For compactness the twelve F-F's required are selected from the total complement of three DEC-type 4215 logic cards, though a certain amount of indirect flow, and attendant cross-connection, result from this arrangement.

Starting at the clock input, on the left, the first three F-Fs constitute an 8-state counter. This, together with its associated output circuitry, equivalent to a 3×8 matrix, defines, consecutively, the 8 bits, B_0 through B_7 inclusive, which constitute one data word of 8 bits, or 7 bits and the parity bit.

Table 6. RAFO SDT
DAS analog input voltage vs SDT octal read-out

Use column A for truncated 8-bit words.

Column B is SDT octal read-out.

Use column C for complete 8-bit words.

A	B	C	A	B	C	A	B	C	A	B	C	B	C	B	C	B	C	B	C
0.000	0	0.0000	1.504	40	0.7520	3.008	100	1.5040	4.512	140	2.2560	200	3.0080	240	3.7600	300	4.5120	340	5.2640
0.047	1	0.0235	1.551	41	0.7755	3.005	101	1.5275	4.559	141	2.2795	201	3.0315	241	3.7835	301	4.5355	341	5.2875
0.094	2	0.0470	1.598	42	0.7990	3.102	102	1.5510	4.606	142	2.3030	202	3.0550	242	3.8070	302	4.5590	342	5.3110
0.141	3	0.0705	1.645	43	0.8225	3.149	103	1.5745	4.653	143	2.3265	203	3.0785	243	3.8305	303	4.5825	343	5.3345
0.188	4	0.0904	1.692	44	0.8460	3.196	104	1.5980	4.700	144	2.3500	204	3.1020	244	3.8540	304	4.6060	344	5.3580
0.235	5	0.1175	1.739	45	0.8695	3.243	105	1.6215	4.747	145	2.3735	205	3.1255	245	3.8775	305	4.6295	345	5.3815
0.282	6	0.1410	1.786	46	0.8930	3.290	106	1.6450	4.794	146	2.3970	206	3.1490	246	3.9010	306	4.6530	346	5.4050
0.329	7	0.1645	1.833	47	0.9165	3.337	107	1.6685	4.841	147	2.4205	207	3.1725	247	3.9245	307	4.6765	347	5.4285
0.376	10	0.1880	1.880	50	0.9400	3.384	110	1.6920	4.888	150	2.4440	210	3.1960	250	3.9480	310	4.7000	350	5.4520
0.423	11	0.2115	1.927	51	0.9635	3.431	111	1.7155	4.935	151	2.4675	211	3.2195	251	3.9715	311	4.7235	351	5.4755
0.470	12	0.2350	1.974	52	0.9870	3.478	112	1.7390	4.982	152	2.4910	212	3.2430	252	3.9950	312	4.7470	352	5.4990
0.517	13	0.2585	2.021	53	1.0105	3.525	113	1.7625	5.029	153	2.5145	213	3.2665	253	4.0185	313	4.7705	353	5.5225
0.564	14	0.2820	2.068	54	1.0340	3.572	114	1.7860	5.076	154	2.5380	214	3.2900	254	4.0420	314	4.7940	354	5.5460
0.611	15	0.3055	2.115	55	1.0575	3.619	115	1.8095	5.123	155	2.5615	215	3.3135	255	4.0655	315	4.8175	355	5.5695
0.658	16	0.3290	2.162	56	1.0810	3.666	116	1.8330	5.170	156	2.5850	216	3.3370	256	4.0890	316	4.8419	356	5.5930
0.705	17	0.3525	2.209	57	1.1045	3.713	117	1.8565	5.217	157	2.6085	217	3.3605	257	4.1125	317	4.8645	357	5.6165
0.752	20	0.3760	2.256	60	1.1280	3.760	120	1.8800	5.264	160	2.6320	220	3.3840	260	4.1360	320	4.8880	360	5.6400
0.799	21	0.3995	2.303	61	1.1515	3.807	121	1.9035	5.311	161	2.6555	221	3.4075	261	4.1595	321	4.9115	361	5.6635
0.846	22	0.4230	2.350	62	1.1750	3.854	122	1.9270	5.358	162	2.6790	222	3.4310	262	4.1830	322	4.9350	362	5.6870
0.893	23	0.4465	2.397	63	1.1985	3.901	123	1.9505	5.405	163	2.7025	223	3.4545	263	4.2065	323	4.9585	363	5.7105
0.940	24	0.4700	2.444	64	1.2220	3.948	124	1.9740	5.452	164	2.7260	224	3.4780	264	4.2300	324	4.9820	364	5.7340
0.987	25	0.4935	2.491	65	1.2455	3.995	125	1.9975	5.499	165	2.7495	225	3.5015	265	4.2535	325	5.0055	365	5.7575
1.034	26	0.5170	2.538	66	1.2690	4.042	126	2.0210	5.546	166	2.7730	226	3.5250	266	4.2770	326	5.0290	366	5.7810
1.081	27	0.5405	2.585	67	1.2925	4.089	127	2.0445	5.593	167	2.7965	227	3.5485	267	4.3005	327	5.0525	367	5.8045
1.128	30	0.5640	2.632	70	1.3160	4.136	130	2.0680	5.640	170	2.8200	230	3.5720	270	4.3240	330	5.0760	370	5.8280
1.175	31	0.5875	2.679	71	1.3395	4.183	131	2.0915	5.687	171	2.8435	231	3.5955	271	4.3475	331	5.0995	371	5.8515
1.222	32	0.6110	2.726	72	1.3630	4.230	132	2.1150	5.734	172	2.8670	232	3.6190	272	4.3710	332	5.1230	372	5.8750
1.269	33	0.6345	2.773	73	1.3865	4.277	133	2.1385	5.781	173	2.8905	233	3.6425	273	4.3945	333	5.1465	373	5.8985
1.316	34	0.6580	2.820	74	1.4100	4.324	134	2.1620	5.828	174	2.9140	234	3.6660	274	4.4180	334	5.1700	374	5.9220
1.363	35	0.6815	2.867	75	1.4335	4.371	135	2.1855	5.875	175	2.9375	235	3.6895	275	4.4415	335	5.1935	375	5.9455
1.410	36	0.7050	2.914	76	1.4570	4.418	136	2.2090	5.922	176	2.9610	236	3.7130	276	4.4650	336	5.2170	376	5.9690
1.457	37	0.7285	2.961	77	1.4805	4.465	137	2.2325	5.969	177	2.9845	237	3.7365	277	4.4885	337	5.2405	377	5.9925

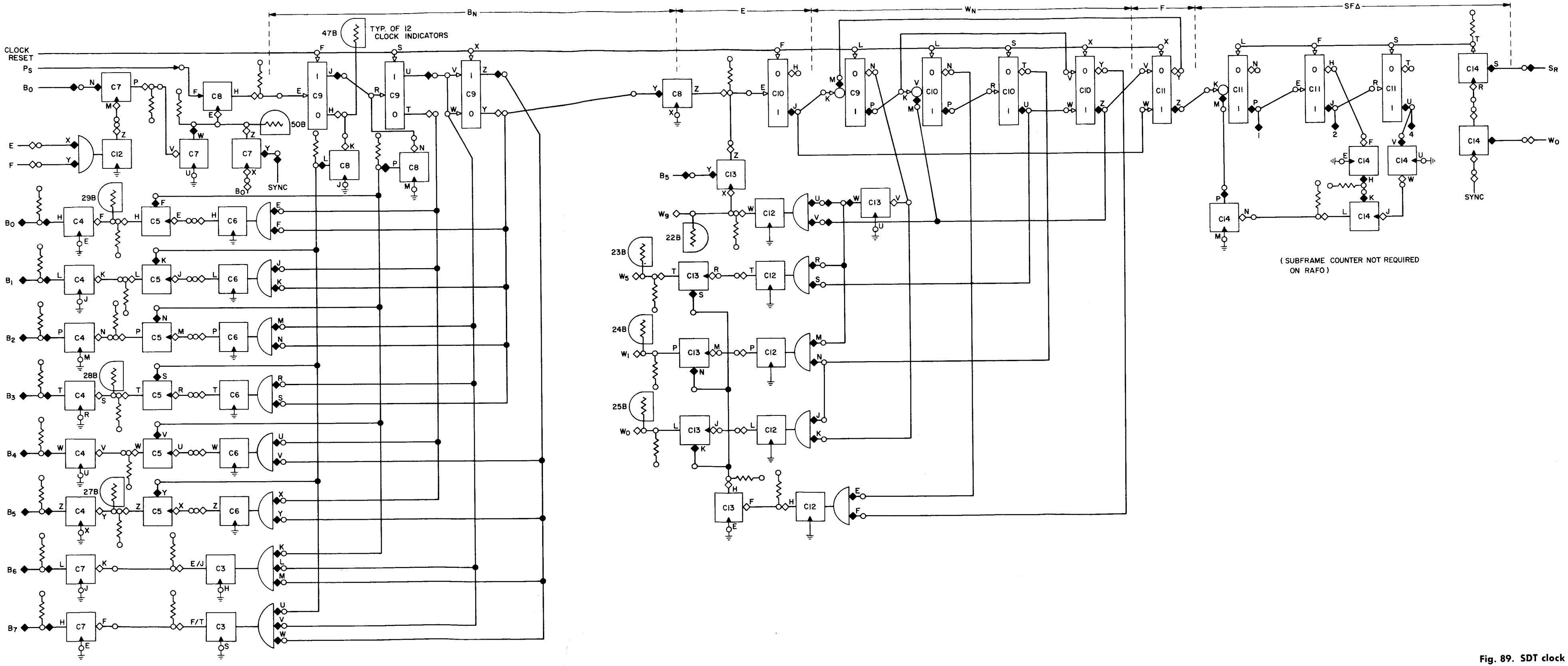


Fig. 89. SDT clock

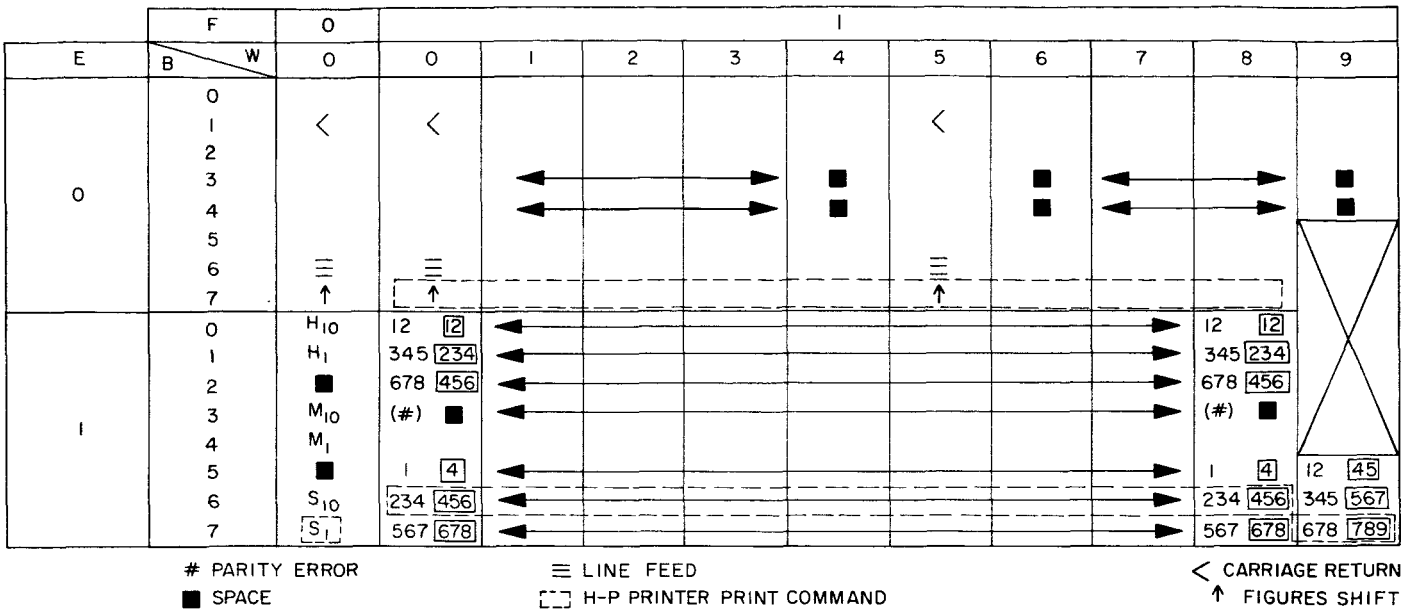


Fig. 90. SDT timing table

Following the bit counter is the single F-F, identified as the "E" F-F, which defines the word whose bits are being counted as *odd* or *even* half of a 16-bit transmitted word. The station of the "E" F-F thus specifies the data word as 8 or 7 bits in length and defines the triplet of a pair, first or second; hence, it controls those functions of the output related to the data word pairing.

Following the "E" F-F, diagrammatically at least, is the 4-bit word counter used to identify, out of its ten possibilities, the four necessary for control of the SDT, W_0, W_1, W_5, and W_9. Note that the "F" F-F, which is shown after the word counter, serves to double the significance of the W_0 output, separating the *time* and *data* read-out functions. At this point, all counting information necessary for control of the SDT has been developed, but the output of the last element of this chain, the "F" F-F, serves as a convenient driving point for the three-element counter used to define the individual subframes.[14]

Detail description of the discrete portions of the clock follows.

Synchronizing gate. In order that the output format truly represent the transmitted data, it is necessary that the DAS and SDT operate synchronously. The method for achieving this is to hold the clock inoperative until its state agrees with the DAS timing. The gating to accomplish this permits shift pulses, the SDT basic timing references, to enter and drive the clock at all times except when the clock is entirely in the *zero* state, that is, $B_0E'F'$. At this time, the shift pulse (P_S) is allowable to enter the clock only if the sync stripper indicates the presence of the 16-bit PN sync word in the input register. Thus, the clock will advance by 1-bit count at the same time that the first bit of the 168-bit scientific data subframe is shifted into the LSB position of the output register.

Drive to the clock may be defined in the following manner:

$$\text{Drive} = P_S[(B_0E'F')' + B_0S_S]$$

where S_S is the sync stripper output.

Bit counter. This portion of the clock employs three complementing F-Fs each having its *one* output connected to the complementing input of the following F-F. Since the assertion level of the output lines from these F-Fs is −3.0 v and the required input to complement them is a positive-going transition, it follows that each F-F will be complemented each time its predecessor changes from the *one* to the *zero* state, at which time the *one* output goes from −3.0 to 0.0 v.

Each stage of a counter of this configuration is thus complemented for every second complementing input to

[14] This subframe identification is not required for *Ranger* Follow-On, since the DAS transmits this along with the data in word 21 of each subframe.

the preceding stage. Obviously, the transitions from one count configuration to the next involve successive changes of sequential stages, or, put another way, the state change of sequential stages propagates through the series at a rate determined by the transition time of individual F-Fs. Such a counter then operates on a strictly asynchronous basis after each input trigger.

Not quite so obvious, but equally important, is the fact that an asynchronous operation of this type may pass through a number of undesired configurations during the transition from one count to the following state. In the case of the transition from 7 to 0, this counter must pass successively through 6 and 4, and each of these states will persist for a time equal to the propagation time through one stage, or 50 nanoseconds in the case of the type 4215 logic card.

For this reason, output signals from this, or any counter of this asynchronous type, must be sampled with a pulse which cannot exist until the counter has reached its new count state. This requirement is met here through use of the read pulse (P_R) which is delayed from the shift pulse (P_S) used to initiate the counting sequence.

"E" F-F. Because the output mechanisms are pulsed at the basic bit rate of 25 bits/sec but actually operate less than 168 times during the period of one scientific data frame, it is convenient to separate information read-out from other functions while still maintaining the SDT basic pulse rate synchronous with the DAS bit rate.

The method of accomplishing this is shown in the timing table, Fig. 90, in which it can be seen that the "E" F-F is used to separate the 16-bit interval into two 8-bit halves, the bit counter having a scale of eight. The first half of the 16-bit transmission word contains one data word, 8 bits in length, which will always be an *odd*-number data word. The last half of a 16-bit transmission word contains the *even*-number data word, 7 bits long, and the parity bit. The effect of the "E" F-F thus becomes identification of the first, odd, half or the last, even, half of the 16-bit transmission word.

In all cases, except word 9 (W_9) the complement action of the "E" F-F occurs when the bit counter goes from state 7 to state 0. This is accomplished by taking the *zero* output, −3.0-v assertion level, of the third stage of the bit counter through an inverter to the complement input of the "E" F-F. Thus, the transition from the *one* to the *zero* state of the bit counter F-F results in a negative-going signal at its output which, when inverted, becomes the required positive-going state change to trigger the "E" F-F.

Use of a common load resistor for the two inverters driving the "E" F-F results in a logical *or* function; that is, either one can raise the common point from −3.0 to 0.0 v. This arrangement is used to accomplish the state change of the "E" F-F shown in the W_9 column of Fig. 90.

By the time the clock advances from B_0 through B_4 in W_9, the most significant bit of the last data word will have been shifted to stage 4 of the output register. Since this is an 8-bit word, it is necessary to obtain read-outs from register stages 4 through 9. The "E" F-F is complemented to the *one* state during the B_4 to B_5 transition and restored to the *zero* state during the B_7 to B_0 transition.

The intermediate complement input to the "E" F-F is derived from the second inverter, which is used to *and* the W_9 and B_5 signals.

Word counter and "F" F-F. The word counter, like all other elements of the SDT clock, makes use of the F-Fs in DEC-type 4215 logic cards. In this particular case, the inhibit gate associated with one of the four F-Fs on a 4215 card is used to meet the required count configuration.

Referring to Fig. 90, it can be seen that the word counter is used to control the output of data from the DAS on the spacecraft. Since the first 16-bit word contains only synchronizing information, the word counter is left in its *zero* state for both the first and second transmission words. The differentiation between these is made by the "F" F-F, which is in the *zero* state during the first, non-data interval and in the *one* state for the remainder of the 168-bit frame, during which significant data are being transmitted.

The sequence of states for the word counter and the "F" F-F is shown in Fig. 91, together with the related "E" F-F, inasmuch as it, too, is necessary to describe the full counting cycle.

Note that the inhibit gate on the "1" F-F of the word counter is used in conjunction with the *zero* output of the "F" F-F to hold the W_0 count through science data word 4. The inhibit gate on the "2" F-F of the word counter is used to hold the "2" F-F in the *zero* state during the W_9 to W_0 transition, at which time the "1" F-F goes from *one* to *zero*. This change complements the

SCIENCE DATA WORD	E	WORD COUNTER					F
		1	2	4	8	W_N	
1 (SYNC)	0	0	0	0	0	0	0
2	1	0	0	0	0	0	0
3	0	0	0	0	0	0	1
4	1	0	0	0	0	0	1
5	0	1	0	0	0	1	1
6	1	1	0	0	0	1	1
7	0	0	1	0	0	2	1
8	1	0	1	0	0	2	1
9	0	1	1	0	0	3	1
10	1	1	1	0	0	3	1
11	0	0	0	1	0	4	1
12	1	0	0	1	0	4	1
13	0	1	0	1	0	5	1
14	1	1	0	1	0	5	1
15	0	0	1	1	0	6	1
16	1	0	1	1	0	6	1
17	0	1	1	1	0	7	1
18	1	1	1	1	0	7	1
19	0	0	0	0	1	8	1
20	1	0	0	0	1	8	1
21	0 / 1	1	0	0	1	9	1
1	0	0	0	0	0	0	0

* DURING F = 0, OUTPUT OF THE SDT IS STATION TIME; WHILE F = 1, OUTPUT OF THE SDT SCIENCE DATA.
STATE CHANGE OF "E" F-F OCCURS AT THE $B_7 \rightarrow B_0$ TRANSITION AND ALSO $B_4 \rightarrow B_5$ TRANSITION IN W_9 (SCIENCE DATA WORD 21).

Fig. 91. SDT clock sequence

"2" F-F unless inhibited by the "8" F-F being in the *one* state.

Inputs to the *one* and *zero* sides of the "F" F-F are separate, making it possible to set this F-F to the *one* state with the *one→zero* transition of the "E" F-F and to the *zero* state with the *one→zero* transition of the "8" F-F.

As can be seen in Fig. 90, it is not necessary to develop all nine output possibilities from the word counter. The four required outputs (Fig. 89), W_0, W_1, W_5, and W_9, are developed in an equivalent 4 × 4 matrix.

These four word outputs are combined with the "E" and "F" F-Fs and the eight B outputs of the bit counter to define the times at which read-out or functional operations are performed, in accordance with the requirements of Fig. 90.

Subframe counter. While not involved in logical timing and/or control, the subframe counter is properly discussed at this point, being a function extension of the timing clock.

The subframe counter is used to count passage of complete science data subframes, is reset to *zero* at master frame, and generates the binary information read out as the octal digit preceding the third data word on the upper line of the hard-copy SDT output for the *Mariner*.

Complement input to the first of the three stages in this counter is derived from the *one→zero* transition of the "F" F-F, which occurs at completion of the processing of the last word of a subframe. Input to the "1" F-F of the subframe counter is through its associated "inhibit" gate, which is closed when the counter reaches a count of 6. The effect of this arrangement is to output a number 6 for each successive data frame of the hard copy. Significance of the appearance of the number 6 is that no master frame has been detected in the incoming data, an anomaly in *Mariner* data, but a normal condition for *Ranger* Follow-On application of the SDT.

The count sequence of the subframe counter, assuming that the master frame does occur, will progress from 0 in master frame through 5 in the sixth consecutive frame after master frame. At the start of the ensuing frame, the count will advance to 6. However, when data words 5 and 6 stand within the input register, the same PN sequence used for synchronizing will exist, since it is transmitted in these positions to identify a master frame. When the sync stripper output is *true* at this time, B_0 of W_1 in the SDT clock, the read pulse (P_R) is logically *and*ed to reset the subframe counter. Thus, the counter output, when subsequently read out at B_5 time, will be zero, which number will immediately precede the octal read-out of the PN sequence, $016\ 145_8$.

A subframe counter is included in the *Ranger* Follow-On (RAFO) DAS. The condition of this 3-bit counter is presented as the least significant octal character of word 21 from the DAS serial transmission. Therefore, this SDT has been modified to inhibit the read-out of its subframe counter.

Since the PN sequence is not presented in words 5 and 6 of the master frame from the RAFO DAS, the RAFO

SDT subframe counter will advance to the number 6 and remain in that state.

Logic drive. As noted at the beginning of the discussion relative to operation of the complete clock, the basic timing increment is the bit duration of the spacecraft DAS. This rate is 25 bits/sec. Pulses defining the beginning of each data bit are generated within the DAS. These pulses, 20 ms in width, appear on the bit sync line of the decoder after the *data* and *data* outputs of the decoder are set to the *one* or *zero* condition of the data.

Development of the clock logic drive is shown in Fig. 92. The bit sync output from DAS is connected to a DEC-type 4504 inverter. This converts the +6/0 v logic levels of the DAS to −3/0 v logic levels for the SDT.

An integral oscillator is available for driving the SDT at the normal rate for troubleshooting purposes and checking for proper operation without an external source.

For even more deliberate operation, particularly when loading the SDT manually, a pushbutton is provided as a source of driving signals. The energizing and filtering networks for this pushbutton are contained in a type 4410 logic card associated with the input drive requirements.

The negative pulse constituting the logic drive signal, regardless of source, is fed to an inverter which is used as part of an *or* gate. The high-level output from this gate is fed through an inverter to one 4410 pulse generator logic card and directly to a second 4410 logic card. Since these cards are characterized by producing an output pulse whenever the input level goes from $\simeq$ 0.0 to $>$ −3.0 v, the first 4410 will produce an output at the leading edge of the input pulse and the second 4410 will produce on output at the trailing edge of the input pulse. The leading edge pulse is used to shift data in both the input and output registers, as well as drive the clock, and is identified as the shift pulse P_S. The trailing edge pulse is used to control the various reading functions, after the system has stabilized from the P_S pulse. It is identified as the read pulse P_R.

Since the read function must provide for the slower operating characteristics of the read-out mechanisms, a DEC-type 4301 delay module is associated with the P_S function. This delay card has two outputs, one of which is a −3.0-v level lasting for the duration of the delay interval, at the end of which time a standard pulse signal is produced at a different output point. The delay interval signal is considered to be S_R for logic development, while the pulse at the end of the S_R interval is identified as ΔP_R.

Since it is difficult to monitor the standard pulses because of their short duration (400 nanoseconds), an alternate source of both P_S and P_R is provided. Two panel-mounted pushbuttons, with integral magnetic *one-shot* structures, are available for switching into the circuit. These make it possible to verify operation of the other elements of the SDT when either, or both, of the 4410 pulse generators are suspect.

As an added convenience, for trouble-shooting facility, a pushbutton *one-shot* is provided to reset all the clock F-Fs to the *zero* state.

When the SDT is connected to data display, the DAS bit sync is not available. Instead, a 400-cycle square wave in synchronization with *data* is presented. In this mode of operation, the SDT generates bit sync by dividing the 400 cycle by 16. This is achieved by the four F-Fs on a DEC-4215 logic card. This counter is reset whenever the *data* line goes from 0 to −3 v, which keeps the counter in sync with the data.

3. TTY Read-out Logic

The functions performed within this area of the SDT include selection of the appropriate binary bits of data, or time, for numerical read-out in octal or BCD notation, respectively, converting this numerical information to TTY 5-bit code, adding the necessary machine operation codes, and delivering this in form suitable for use by the output mechanism.

Numerical data are obtained from two sources, the output register on the station clock, and additionally the parity error symbol requirement is determined from the state of the parity error storage F-F.

Selection of the proper source for reading out and the necessary bit positions within the source area is entirely a function of timing relative to the serial progress of data through the SDT—as are all the formating machine operations of the output mechanism.

The relationships of the data and the timing are shown, diagrammatically, in Fig. 85. The specific functions to be performed at each bit time are tabulated in Fig. 90 to result in an output format of the appearance of Fig. 87.

Basically, the read-out function is performed in two discrete, but simultaneous, operations. The first of these

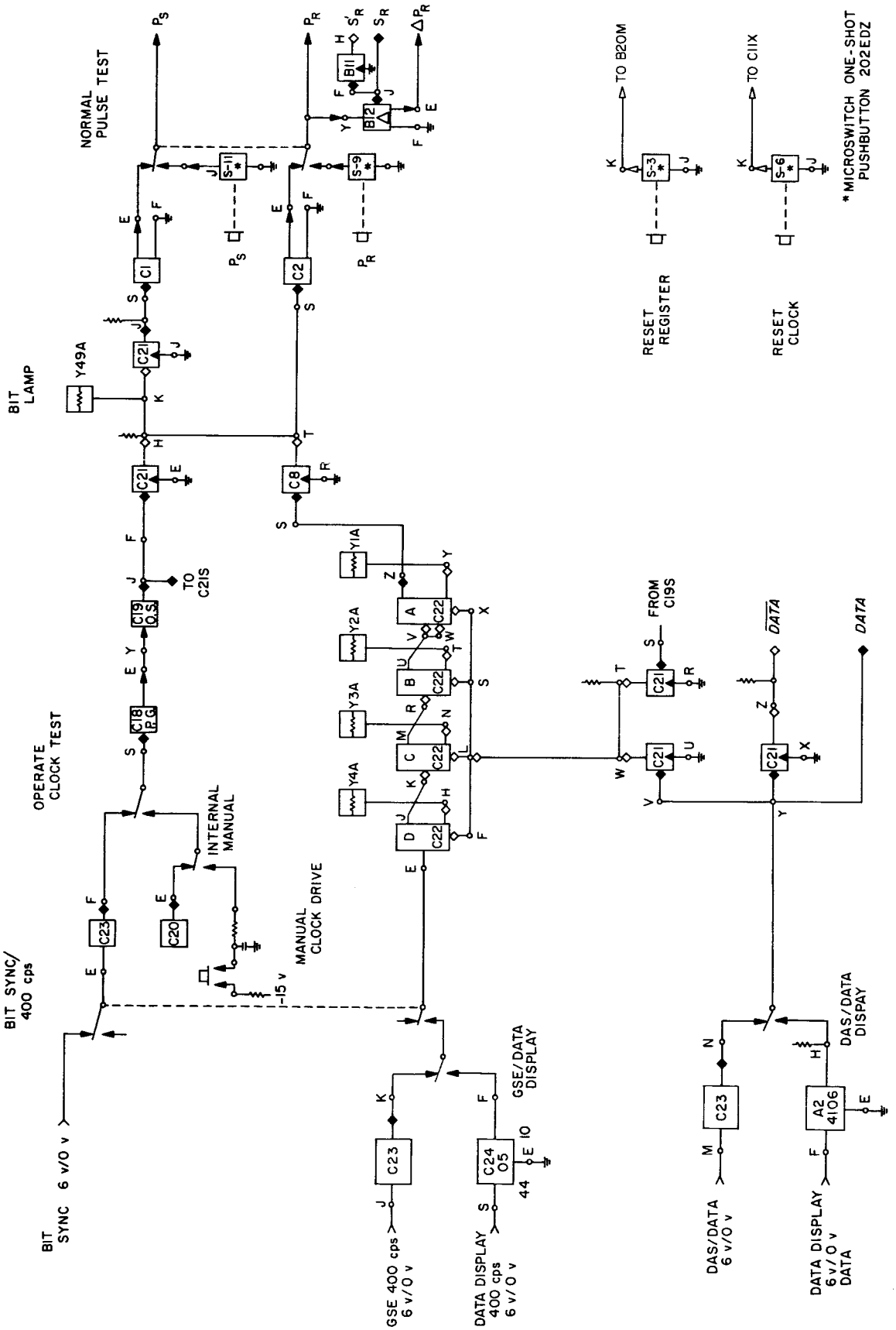


Fig. 92. SDT clock logic drive

is the read-out to octal, or BCD, form. The second is the conversion of these to TTY code.

To simplify the explanation of the following combinational functions, their operation will be described by switching logic equations. Mechanization can be determined by consulting the appropriate diagrams.

a. TTY readout and function control. Functional requirements of the output mechanism, differentiated from numerical information read-out, include:

$$\# = EF\,B_3\,(\text{parity})$$
$$^{15}\square = E'\,[(W_0 + W_5)'\,(B_3 + B_4)] + EF'\,(B_2 + B_5) + EF\,B_3$$
$$^{15}< = E'\,(W_0 + W_5)\,B_1$$
$$^{15}\equiv = E'\,(W_0 + W_5)\,B_6$$
$$\uparrow = E'\,(W_0 + W_5)\,B_7$$

Numerical data includes read-out of selected bit positions of the output register or station time input lines. The positions are here grouped as necessary to constitute desired octal or BCD information.

$$12 = (EF\,W_9')\,B_0$$
$$234 = (EF\,W_9')\,B_1$$
$$456 = (EF\,W_9')\,(B_2 + B_6)$$
$$4 = (EF\,W_9')\,B_5$$
$$678 = (EF\,W_9')\,B_7$$
$$45 = (EF\,W_9)\,B_5$$
$$567 = (EF\,W_9)\,B_6$$
$$789 = (EF\,W_9)\,B_7$$

Read-out inhibit =

$$E' + F'(B_2 + B_5) + F(B_3 + B_4)$$
$$H10 = B_0\,E\,F'$$
$$H1 = B_1\,E\,F'$$
$$M10 = B_3\,E\,F'$$
$$M1 = B_4\,E\,F'$$
$$S10 = B_6\,E\,F'$$
$$S1 = B_7\,E\,F'$$

Reference to Fig. 93 will show the mechanization of the functional and read-out requirements, in accordance with the foregoing equations.

[15] Since these three functions are represented by a single hole, in TTY code, their output inverters may be ored in the TTY matrix.

b. TTY numeric readout. As noted previously, numeric data are read from selected bit positions of the output register or the station time. This read operation consists of *and*ing the read-out control functions and the appropriate data lines to generate octal-BCD digits 1_8, 2_8, 4_8, and 8_8. All these *and* operations are performed by two-input negative *and* gates, six of which make up one DEC-type 4113 logic card.

Figure 94 shows the mechanization of these operations. It should be noted that both the assertion and negation outputs are developed in *down* logic, to meet the requirements of the octal-BCD/TTY conversion process.

c. Octal-BCD/TTY conversion. Operation of this function is shown in Fig. 95. The matrix-type portions of this diagram require no particular explanation.

Also shown is the method used to inhibit the drive to the output mechanism during the time no data read-out or machine operation is occurring.

d. Digital recorder numeric readout. The numeric data to the digital recorder are read from bit positions 2 through 9 of the output register. All bit positions are fed through DEC-type 4667 inverters which convert the −3/0 v logic levels to 0/−15 v. The latter logic levels are compatible with the +1248 code column boards in the digital recorders (see Fig. 96).

All lines are connected in parallel to the digital recorder, where BCD to decimal conversion is performed. Bit positions 7 to 9 are decoded as the least significant digit of the three-digit print-out; bit positions 4 to 6 are decoded as the second digit; and bit positions 2 and 3 are decoded as the most significant digit. The logic associated with bit position 2 inhibits the read-out of this position during *even word* print-out. This limits the maximum read-out for even words to 177.

Similar logic is shown associated with the parity error column. This provides for printing a minus sign for parity error only along with the odd words.

During data read-out, the "1" reference level output is at 0 v and the "0" reference level output is at −15 v. These levels are required for the +1248 code column boards in the digital recorder.

The two reference levels are also connected to the six −1248 code column boards associated with the time read-out. The levels are just the opposite required for

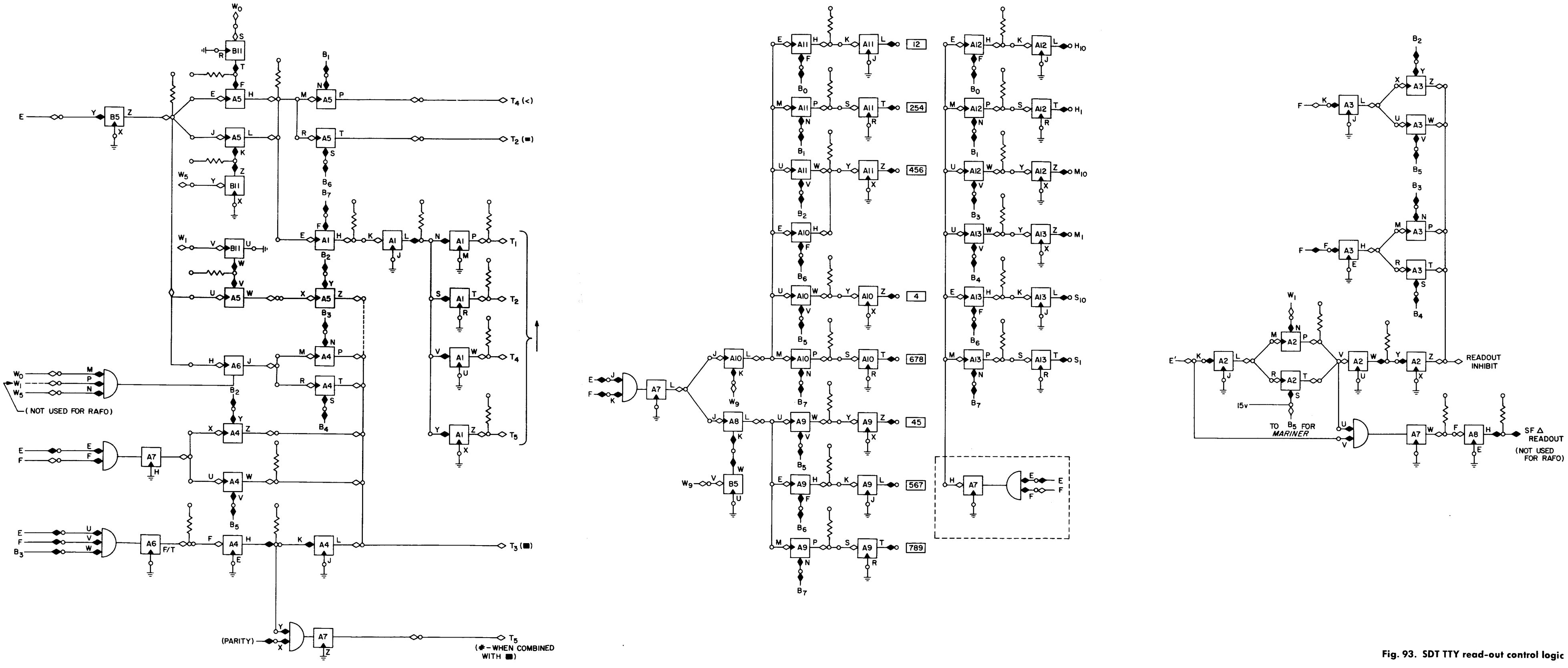


Fig. 93. SDT TTY read-out control logic

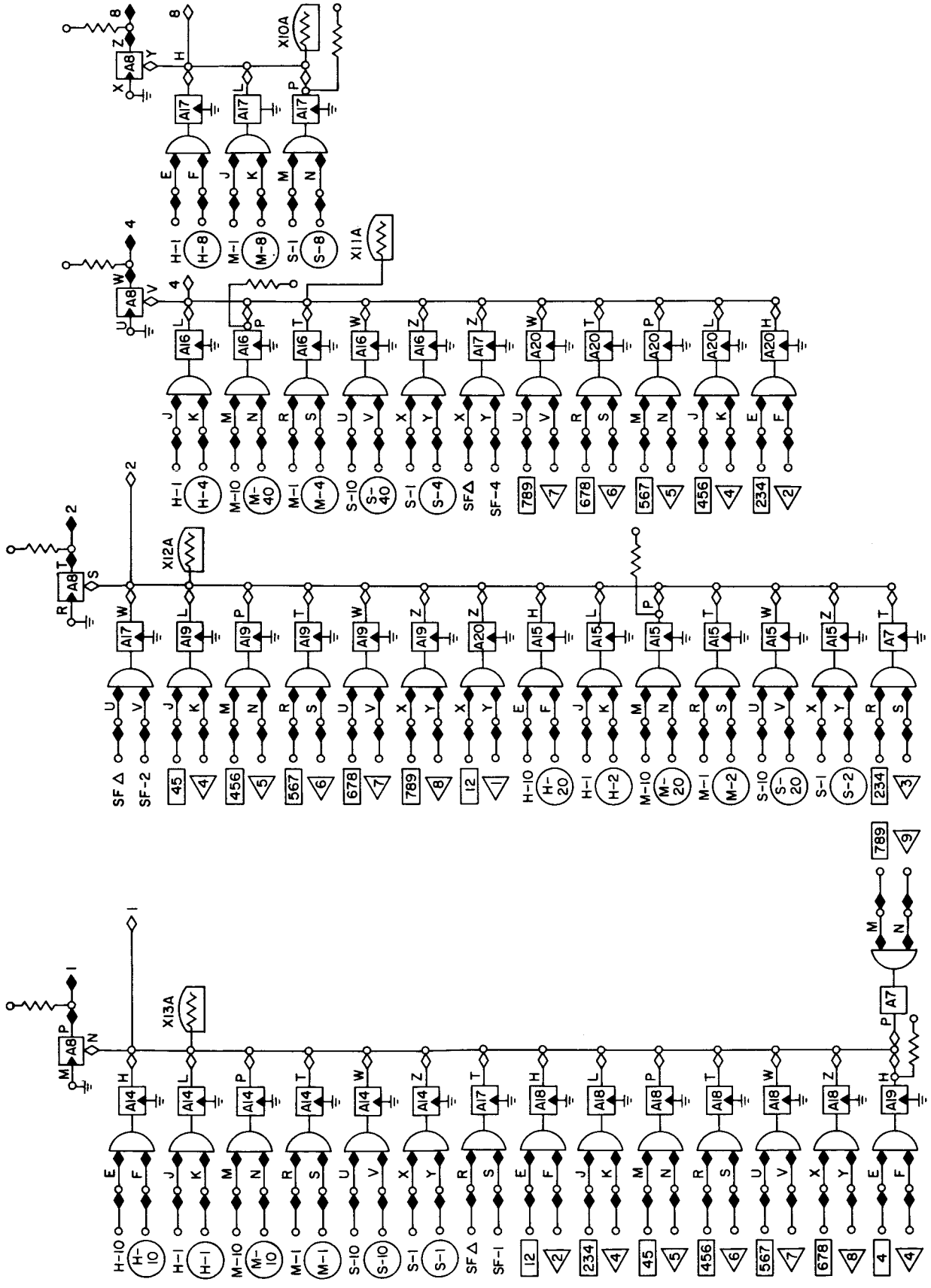


Fig. 94. SDT TTY numeric read-out

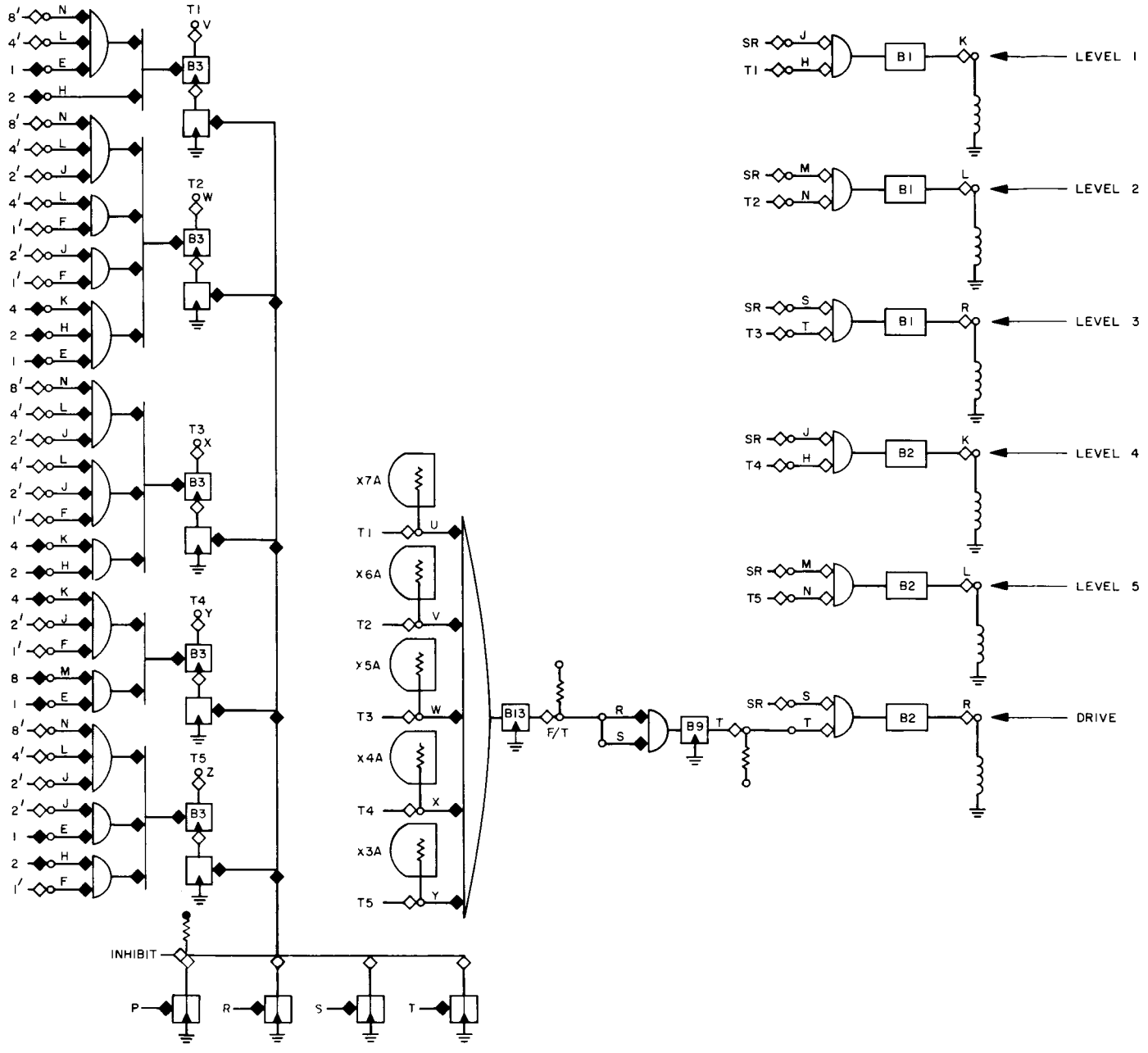


Fig. 95. SDT octal-BCD/TTY converter

these boards. The logic of the boards is such that this condition causes *blanks* to be printed in the columns regardless of the logic levels on their input lines.

When time is to be printed, the two reference lines change state. This causes *blanks* to be printed in the data columns and now allows time to be printed in its column.

e. Digital recorder readout control. The digital recorder read-out is achieved merely by generating a *"print"* command to the recorder during the clock time when the data are contained in bit positions 2 through 9 for the odd words and 3 through 9 for the even words. Time is printed at the same instant the *units* character of seconds is punched on the TTY tape.

The functional requirement for the print command is:

$$S_R\,(F'EB_7 + FE'B_7 + W'_9FEB_6 + W_9FEB_7)$$

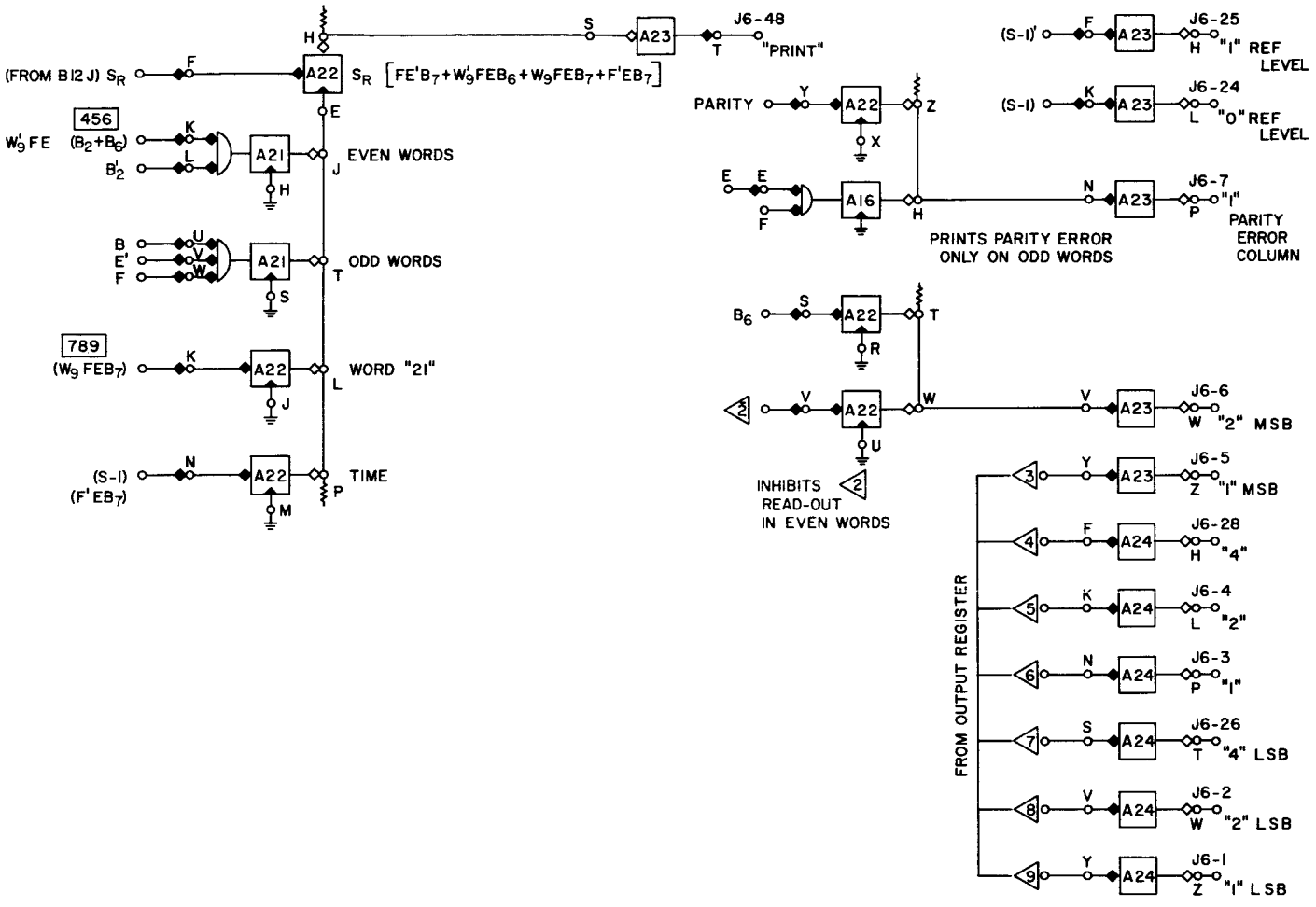


Fig. 96. Digital recorder numeric read-out and read-out control

where $F'EB_7$ = time print-out

$FE'B_7$ = odd word print-out

$W_6'FEB_6$ = even word print-out

W_9FEB_7 = word 21 print-out

Reference to Fig. 96 will show the mechanization of the functional and read-out requirements, in accordance with the foregoing equation.

C. Operation

Normal *on-line* operation of this equipment requires no attention from the associated personnel beyond establishing that the SDT is ready to accept data. This condition is verified by noting that the *"circulate"* switches are *off* (white) and that the *"clock test-operate"* switch is in the *"operate"* condition. The three toggle switches shall all be switched to the left for data entry from the DAS and to the right for data entry from data display.

XVII. SYSTEM TEST OPERATION

The *Ranger* Follow-On system test covers three operations: subsystem, system, and environment. The subsystem and system tests are performed at JPL and AMR, whereas the environmental test is performed only at JPL. The subsystem and system operations as applied to the scientific experiments will be discussed individually.

A. Subsystem Test

The purpose of this test is to integrate all the instruments on the spacecraft into a flight configuration and use the GSE for verification of this condition. This is the first time that the interface between the GSE and the individual instruments is verified. A definite sequence is followed in order to evaluate the compatibility between instruments and between each instrument and the GSE. Following are the checkout procedures for the cabling and each instrument.

1. Cabling

All the cabling was previously verified by a continuity check. Experiment power is verified at every connector before power is applied to any experiment. Each experiment in turn is connected into the flight harness; then power is applied and outputs are verified until the entire subsystem is intercabled and verified. Table 7 gives the power supply voltage for each experiment.

2. Ion Chamber and Particle Flux

A block diagram of the checkout of these instruments is shown in Fig. 97. The test sequence is as follows:

1. A known radioactive source, cobalt-60, is installed near the instrument.
2. The instrument is turned on and power is monitored and compared with previously established tolerances.
3. The particle flux digital outputs are sampled for 1 min and printed out as a decimal number. The elapsed time between ion chamber pulses rather than the number of pulses is printed out on the same printer.

3. Cosmic Dust Experiment

The block diagram of the checkout of this instrument is shown in Fig. 98. The test sequence is as follows:

Table 7. Power supply voltages of the experiments

	Experiment	Voltage	Tolerance, v
1	Particle flux	6	±1
2	Particle flux	15	±1
3	Electron flux	6	±1
4		− 6	±1
5		2	±0.5
6		20	±1
7	Cosmic dust	3	±0.5
8	Cosmic dust	6	±0.5
9	DAS	6	±0.5
10		− 6	±0.5
11		12	±0.5
12	Magnetometer	20	±0.05
13	Low-energy ion	12	±1
14	Low-energy ion	−45	±1
15	Electron-proton spectrometer	16	±0.5
16		16.95	±0.05
17		16.00	±0.05
18		28	±0.5
19	Low-energy plasma	6	±0.3
20		6	±0.3
21		− 6	±0.3
22		− 6	±0.3
23		12	±0.3
24		12	±0.3

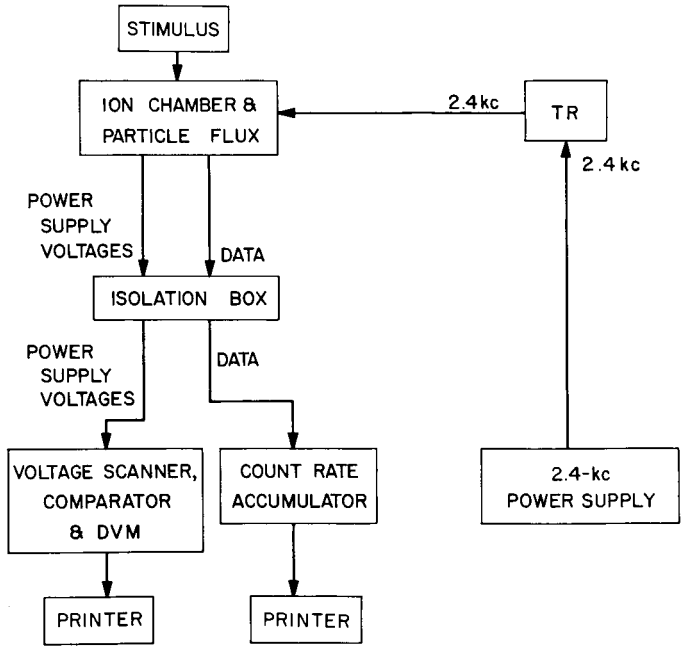


Fig. 97. Ion chamber and particle flux detector checkout block diagram

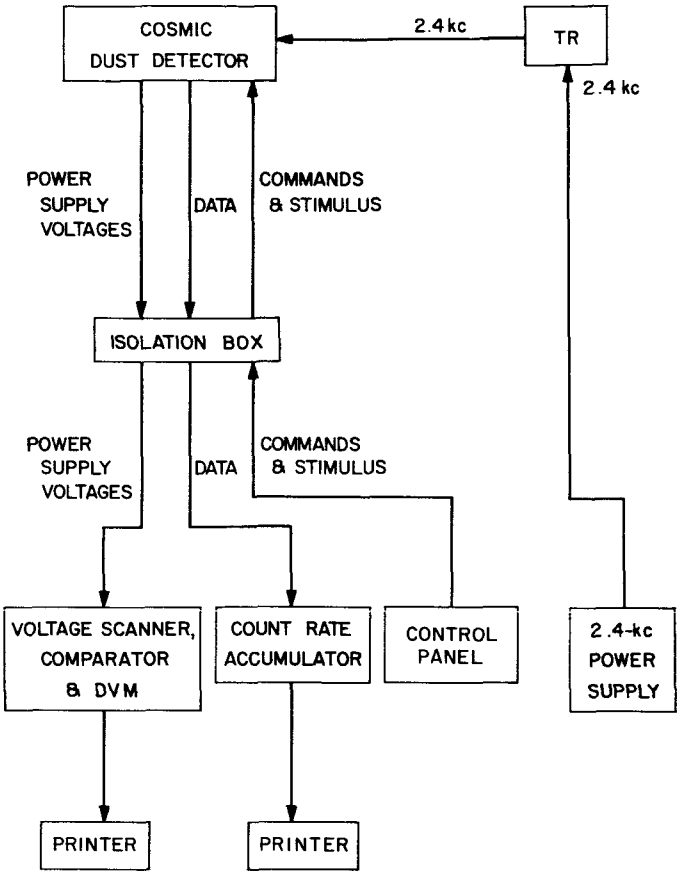


Fig. 98. Cosmic dust detector checkout block diagram

1. The instrument is turned on and power is monitored and compared with previously established tolerances.
2. The number and intensity of stimulated impacts are selected. A reset command is then sent to the experiment and all the flip-flops are reset.
3. A definite time after the experiment is reset, the simulated impacts set the flip-flops to correspond to the information received.
4. One sec after the flip-flops are set, the experiment output is recorded in binary form on a printer. Figure 99 shows a relative timing sequence between events.
5. The intensity and the number of impacts are varied, and the procedure is repeated in order to completely check out the experiment.

4. Search Coil Magnetometer Experiment

A block diagram of the checkout of this instrument is shown in Fig. 100. The test sequence is as follows:

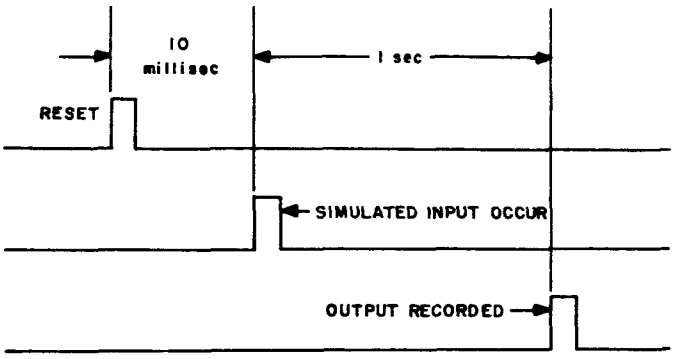


Fig. 99. Cosmic dust detector checkout timing sequence

1. The instrument is turned on and power is monitored and compared with previously established tolerances.
2. An inflight calibrate-off command is sent to the experiment.
3. The magnetometer is commanded into a high-scale and low-scale mode by the GSE, and the outputs are recorded on a printer for each condition.
4. An inflight calibrate-on command is sent to the experiment by the GSE.

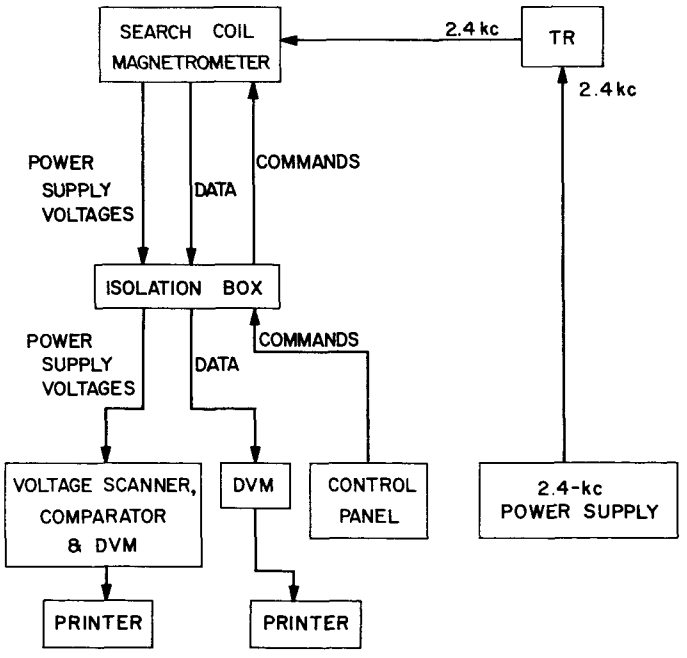


Fig. 100. Search coil magnetometer checkout block diagram

5. The magnetometer is commanded into a high-scale and low-scale mode by the GSE, and the outputs are recorded on a printer for each condition.
6. The magnetometer is checked out with a probe both enabled and disabled to ensure output compatibility.

5. Low-Energy Plasma Experiment

A block diagram of the checkout of this instrument is shown in Fig. 101. The test sequence is as follows:

1. The instrument is turned on, and power is monitored and compared with previously established tolerances.
2. A simulated current is injected into the experiment, and the outputs are recorded on a printer.
3. Ten step commands are initiated by the GSE with outputs of the experiment recorded on the printer after each command.
4. The simulated input current is increased through four additional steps with each step verified exactly as the first.

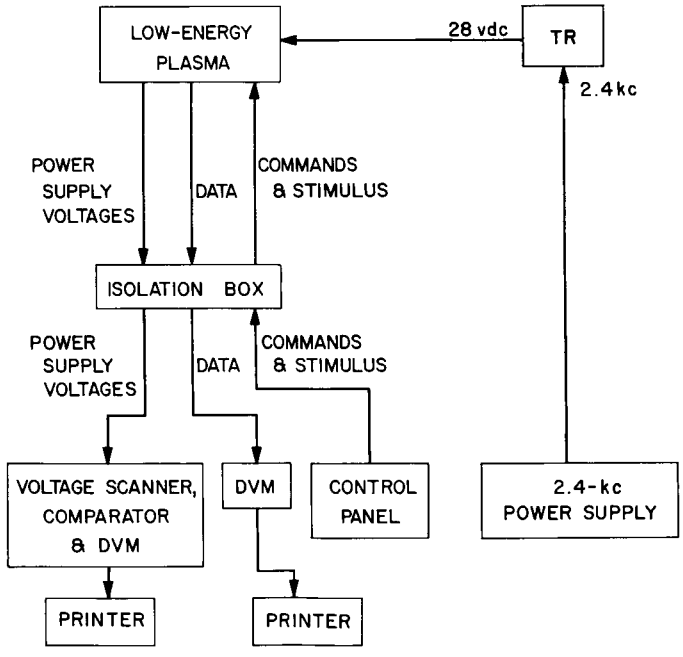


Fig. 101. Low-energy plasma probe checkout block diagram

6. The Low-Energy Ion Detector Experiment

A block diagram of the checkout of this instrument is shown in Fig. 102. The test sequence is as follows:

1. The instrument is turned on, and power is monitored and compared with previously established tolerances.
2. Simulation current to the electrometer is injected through the current probe, and the output is recorded on a printer.
3. The experiment is sequenced through 120 steps by commands from the GSE. The analog output is recorded on a printer after each sequence command, while the amplifier reference voltage is continuously recorded on the Visicorder.
4. Electrometer input current is increased through six more steps, while the experiment is sequenced and monitored after each step in exactly the same way as for step 1.

7. Electron-Proton Spectrometer Experiment

A block diagram of the checkout of this instrument is shown in Fig. 103. The test sequence is as follows:

1. The instrument is turned on, and power is monitored and compared with previously established tolerances.
2. A known radioactive source, cesium 137, is installed near the instrument.

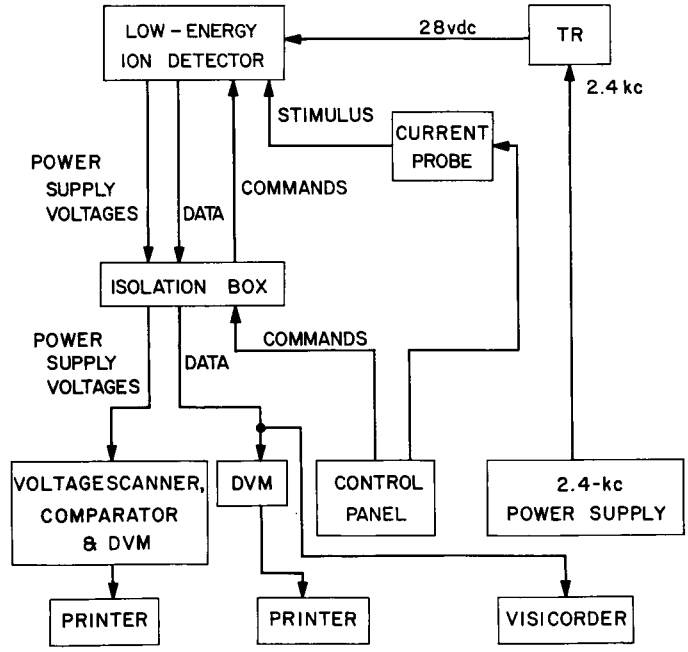


Fig. 102. Low-energy ion detector checkout block diagram

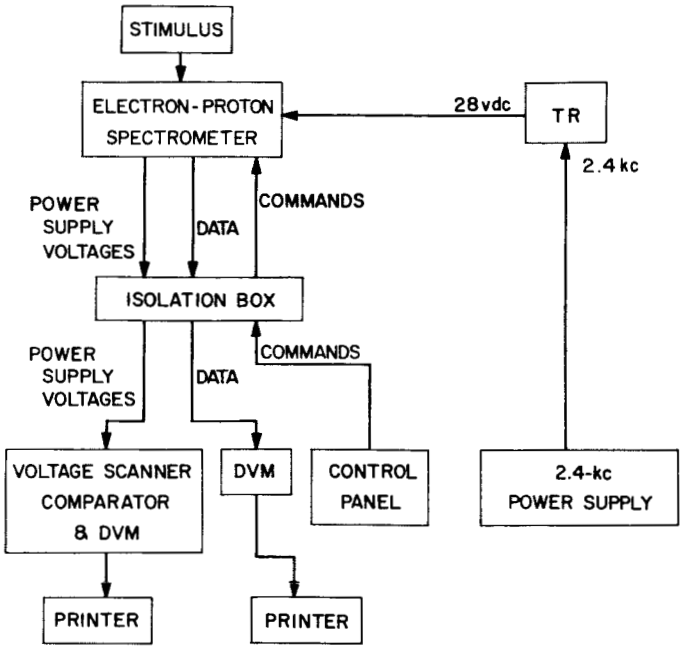


Fig. 103. Electron-proton spectrometer checkout block diagram

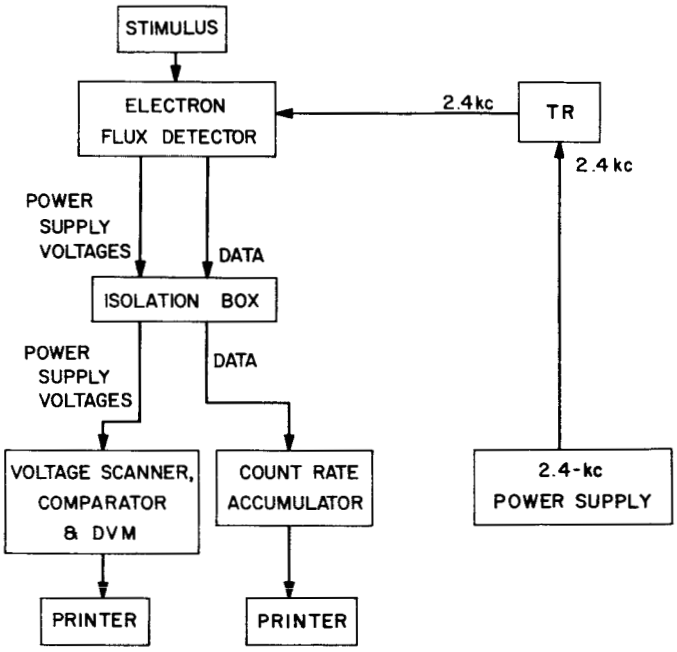


Fig. 104. Electron flux detector checkout block diagram

3. The experiment is given 10 sequence commands by the GSE. After each command, the experiment output is recorded on a printer.

4. The cesium-137 is replaced by a polonium-210 radioactive source.

5. The experiment is again given 10 sequence commands by the GSE with the data output recorded on a printer as before.

8. Electron Flux Detector Experiment

A block diagram of the checkout of this instrument is shown in Fig. 104. The test sequence is as follows:

1. The instrument is turned on, and power is monitored and compared with previously established tolerances.

2. Calibrated sources are installed near the experiment detector.

3. The electron flux detector digital outputs are sampled for 1 min and printed out as a decimal number.

9. Data Automation System

A block diagram of the checkout of this instrument is shown in Fig. 105. The test sequence is as follows:

1. The instrument is turned on and power is monitored and compared with previously established tolerances.

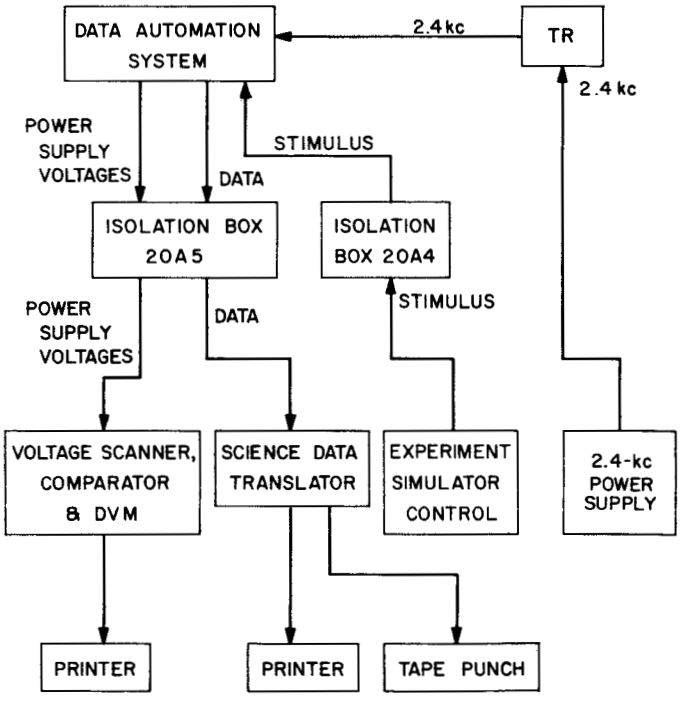


Fig. 105. Data automation system checkout block diagram

2. Digital signals simulating experiment outputs are initiated by the GSE to the DAS one at a time. The binary output from the DAS is decoded by the science data translator, recorded on a printer and punched paper tape, and then compared with the simulated input.
3. Analog signals simulating experiment outputs are initiated by the GSE to the DAS one at a time. The binary output from the DAS is decoded by the SDT, recorded on a printer and punched paper tape, and compared with the simulated input.

After each experiment is checked out individually, all the experiments, including the DAS, are interconnected into a subsystem configuration. A general block diagram of this checkout is shown in Fig. 106. All the experiments are turned on and stimulated, and it is verified that the raw data from each experiment are compatible with the coded data from the DAS. This ensures that all the instruments will function together as a system without any interaction.

B. System Test

After all the subsystems of the spacecraft have been verified, the entire spacecraft is interconnected into a system configuration for interface verification. The first consideration given a system test is to ensure that no interactions exist between spacecraft subsystems. Any discrepancies that appear between the subsystem and system information are investigated thoroughly to ensure that they were due to environmental changes and not to component interactions. A science system checkout procedure is given in an appendix.

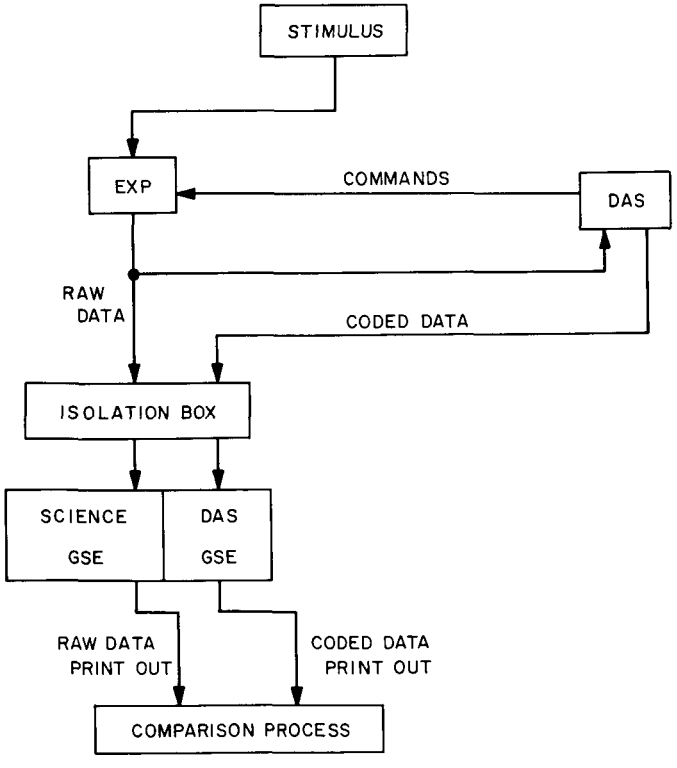


Fig. 106. Subsystem checkout block diagram

Several systems tests of extended length are conducted to ensure information repeatability. The spacecraft is also commanded through a complete operational sequence from launch countdown through spacecraft injection. Data from systems tests are compiled and filed to build a history of operation of the scientific instruments. These records are utilized to gain information about instrument performance at any later date.

C. Environmental Testing

Each experiment is required to pass an individual test before assembly on the spacecraft. Some of the requirements are heat sterilization for 36 hr at 125°C and exposure to ethylene oxide gas mixture for 24 hr. Every experiment is mounted on a test fixture to the output of an electrodynamic vibration exciter. Vibration which simulates actual launch and flight vibrations is then applied to the X, Y, and Z axes. After vibration, each experiment is inspected and bench-checked for functional operation. The final vibration phase is effected with all the experiments mounted on the spacecraft and the entire spacecraft shaken in three mutually perpendicular planes. Verification of spacecraft operation is performed before and after each plane of vibration testing.

The vacuum temperature test simulates as closely as possible the conditions the spacecraft encounters in space flight. This test was conducted in a stainless-steel vacuum chamber approximately 6 ft in diameter and 7 ft high. A cold shroud containing liquid nitrogen and strip heaters placed on various parts of the structure was used for thermal simulation of outer space. The spacecraft is operated in each of the power modes at the appropriate solar intensity to the flight sequence. The operation in each mode takes place in real time and commences with the spacecraft thermally stabilized in the preceding power mode. If the spacecraft is not thermally stabilized at the end of the preceding power mode, the next mode is started with the spacecraft in the changing condition. If the power mode is so long that the spacecraft has completely stabilized before the power mode is ended, the spacecraft is operated only until stabilization. Thermal

design testing consists of verifying that, during operation at power modes of long duration, no temperature on the spacecraft goes above 40 or below 20°C and that, during the operation at power modes of short duration, no temperature on the spacecraft goes above 55 or below 0°C. After the vacuum temperature tests are completed, another system test is performed to ensure that all instruments are still operating within specified tolerances.

ACKNOWLEDGMENT

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BIBLIOGRAPHY

1. *Space Programs Summary 37-17, Vol. VI,* "Ranger Follow-On Scientific Experiments," Jet Propulsion Laboratory, Pasadena, October 31, 1962.
2. *Space Programs Summary 37-18, Vol. VI,* "Ranger Television Camera Subsystems," Jet Propulsion Laboratory, Pasadena, December 31, 1962.
3. Hèntosz, G., *Scientific Subsystems Operation: Mariner R,* Technical Memorandum 33-89, Jet Propulsion Laboratory, Pasadena, July 1, 1962.
4. *Assembly and Operations Plan: Rangers 6, 7, 8, and 9,* Engineering Planning Document 94, Jet Propulsion Laboratory, Pasadena, June 11, 1962.
5. *Instruction Manual and Final Engineering Report: Ranger Follow-On and Data Automation System,* Computer Control Company, Inc., Old Connecticut Path, Franinghan, Mass., November 1962.
6. *Operating Instruction Manuals,* Consolidated Systems Corp., Monrovia, Calif.

Appendix

Ranger Follow-On Spacecraft Science System Checkout

The purpose of this procedure is to provide the science GSE operator with a set of detailed instructions for use in system and subsystem testing of the *Ranger* Follow-On spacecraft. The test sequence is outlined in Fig. A-1. The spacecraft is assumed to be operating in a mode similar to the system test operation.

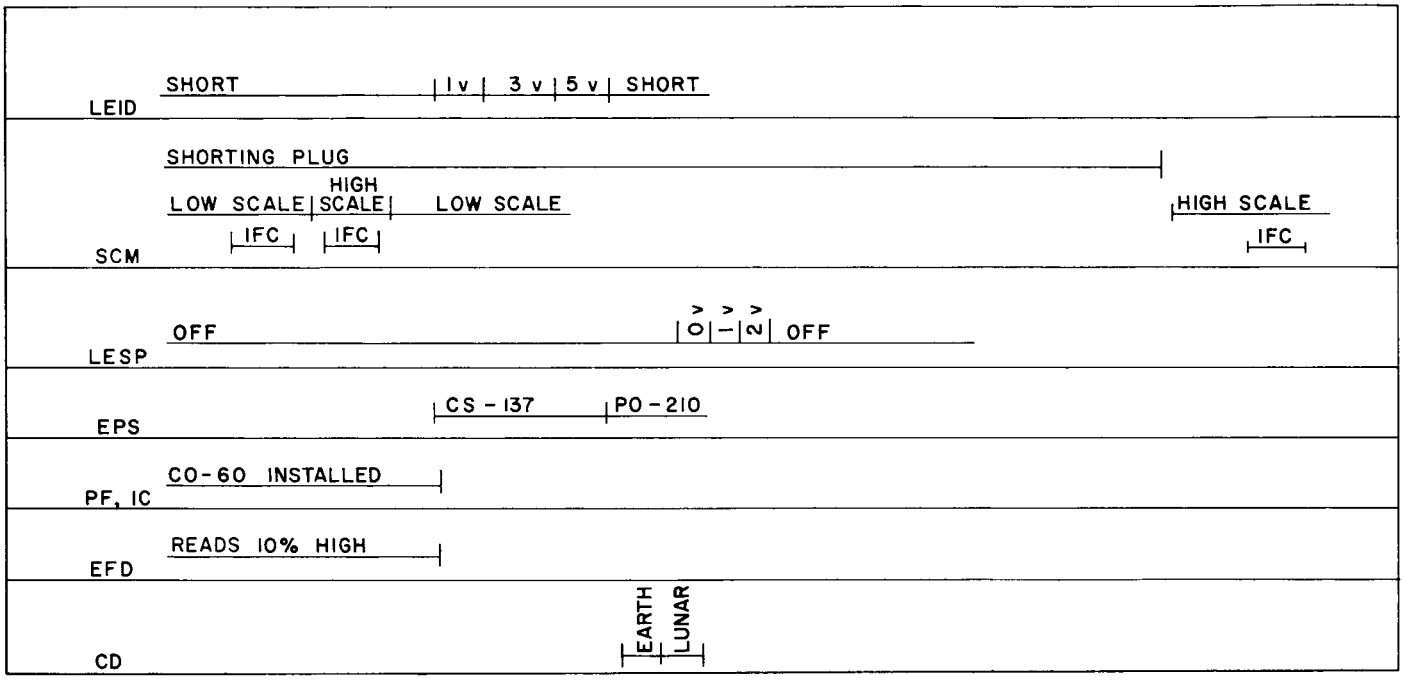

Fig. A-1. Bar graph, science system test

Step	Operation	Normal Indication
1	Install patch panel with the following connections: AE10 to P2 and P6 AE13 to P4 — L10 to D3 AE5 to P8 — L11 to D4 L2 to J7 — L12 to A11 L3 to J6 — L13 to A12 L4 to J5 — L14 to A13 L5 to J4 — L15 to A14 L6 to J3 — L16 to A6 L7 to J8 — L17 to A5 L8 to AC4 — L18 to A4 L9 to AC5 — L19 to A22 L20 to AC7 — L1 to AA9 M1 to S3, S4, S14, S18, T21, T22, AE1, AE2, AE3, AE4, AG4, Q2, Q4, Q6, Q8, Q18, and Q20.	
2	Turn on 60-cycle power. Verify that all GSE equipment is on.	Equipment power on lights is on and spacecraft power indicator light is off.

Step	Operation	Normal Indication
3	See that all controls are set as follows: DVM 1 and DVM 2 a. Range switch to *auto*. b. Auto trigger control set as required. c. Power switch to *auto print*. d. Function switch to dc. e. Mode switch to *auto*. VOLTAGE SCANNER a. Mode selector to *auto*. b. Press *reset* to clear system.	*Auto, start, ready,* and *override* lights are on; all others are off.
	CONTROL PANEL a. *Cosmic dust auto earth cal* and *auto lunar cal* on, and *auto cal pulse selector* to zero. *Hi/Lo* pulse switch to *Lo* pulse. b. *L/E ion electrometer input voltage* to short. c. *L/E plasma binary lock* off, and *electrometer simulated input* off. d. *Magnetometer high scale* off. e. *Test mode* to *DAS commands*. f. Voltage scanner, count rate accumulator control circuits, and SDT power switches on.	*Auto earth cal, auto lunar cal, cal pulse, binary lock off, high scale off, DAS commands, voltage scanner power on, count rate accumulator power on, control circuits power on* and *SDT power on* lights are on; all others are off.
	PRINTER 1 AND 2 *Record* on; mark tapes with test I/D.	Pilot light on.
	COUNT RATE ACCUMULATOR a. *Cosmic dust data, ion chamber data,* and *standby* lights should be off. b. *PF End sens 5, PF Coin 7, PF Stain 1* and *PF Bery 3* or *EF output 3/6, EF output 1/2,* and *EF output 2/4* lights should be on.	
	OSCILLOSCOPE a. With type 72 plug-in installed, jumper channel A input on oscilloscope to channel 1 high input on scope panel. b. With type 63 plug-in installed, jumper plus input on oscilloscope to channel 1 high input on scope panel, and minus input on oscilloscope to channel 1 low input on scope panel.	
	VISICORDER a. *Grid* to 3. b. *Galv* to 4. c. *Timer* to 1. d. *Power* to lamp. e. Operate speed as required.	
	EL PRINTER a. *Record* on. b. *Record* off till A2 is released.	Determine comparison with CRA decades.
	METER PANEL Meter selector switch to SDT.	Meter 1 reads −7.5 v. Meter 2 reads −15 v. Meter 3 reads +10 v.
	EXPERIMENT SIMULATOR CONTROL All switches should be off. H.P. 562 PRINTER *Record on;* mark tape with Test 1/D (rubber stamp). TALLY PUNCH *Power on.* SDT a. "1", "0", *reset register, circulate long, circulate short, reset clock, operate* and *sync* lights should be on; all other lights should be off. b. Press *clock* and *register reset* switches to clear SDT registers. c. *Data* switch in DAS position. d. *Sync* switch in *bit sync* position. e. *400-cycle* switch in GSE position.	

Step	Operation	Normal Indication
4	Press voltage scanner *start* command.	DVM 2 will read and printer 1 will print voltages shown in Table A-1.
5	Press voltage scanner *reset* command.	
	SEARCH COIL MAGNETOMETER	
6	Hold *IFC relay actuate* switch in and press *IFC off* command.	
7	Set analog selector to *300 cps* and press DVM *read* at SF 3, 4, and *5*. Mark these three readings on HP *562* tape.	
8	After MFC has read XX*7*, hold *IFC relay actuate* switch in and press *IFC on* command. Mark HP *562* tape accordingly.	
9	Set analog selector to *3 cps* and press DVM *read*.	
	Set analog selector to *10 cps* and press DVM *read*.	
	Set analog selector to *30 cps* and press DVM *read*.	
	Set analog selector to *100* cps and press DVM *read*.	
	Set analog selector to *300 cps* and press DVM *read*.	
	Set analog selector to *scale* and press DVM *read*.	
10	After MFC has read XX*7*, press *high scale on* switch.	
11	Set analog selector to *scale* and press DVM *read*. Determine if magnetometer went to high scale.	
12	After MFC has read XX*7*, hold *IFC relay actuate* switch in and press *IFC on* command.	
13	Set analog selector to *300 cps* and press DVM *read* at S/F 3, 4, and *5*. Mark readings on H.P. tape and record.	
14	After M/F count has read XX*7*, press *high scale off* command.	
	PARTICLE FLUX AND ION CHAMBER CHECKS	
15	Check particle flux and ion chamber for proper counts.	*PF Stain*, about 100,000/min. *PF Bery*, about 100,000/min. *PF Coinc*, about 1000/min. *PF End sens*, about 10,000/min. *Ion Chamber*, 1 pulse each 6 sec.
	ELECTRON FLUX DETECTOR	
16	Change sources—remove Co-60 and install Cs-137. Note change on EI tape, H.P. tape.	
17	Check EFD for proper counts for particular instrument.	Less than 3000/min.
	LOW-ENERGY ION DETECTOR	
18	Examine data obtained with input to probe on *short*. Take analog readings and compare with DAS readout. Record.	
19	Turn Visicorder on, speed 0.1 in/sec, LEID amp reference on channel 20, LEID scale on channel 18.	
20	Set electrometer input voltage to 1 volt. Note M/F count and leave 1-volt input on for at least 10 M/F counts. Mark H.P. tape and analog tape.	
21	Take analog reading and compare with DAS readout. Record both readings.	
22	After 10 M/F counts, switch electrometer input voltage to 3 volts. Note M/F count. Mark voltage change on analog and H.P. tape.	
23	Take analog readings and compare with DAS readout. Record both readings.	
24	After 10 M/F counts, switch electrometer input voltage to *5* volts. Note M/F count. Mark voltage change on analog and H.P. tapes.	
25	Take analog readings and compare with DAS readout. Record both readings.	
26	After 10 M/F counts, switch electrometer input voltage to short. Note change on H.P. tape.	
27	During steps 21, 23, and *25*, switch analog selector to *LEID scale*. Observe scale changes 0, −10, and −30 volts. Record values.	
	ELECTRON-PROTON SPECTROMETER	
28	Switch analog select switch to *EP spect data*. Push DVM *read* switch during S/F 0, 1, 2, and 3. Mark DAS readout tape. Record and compare analog and DAS tapes. (S/F 4—word 4)	
29	Set analog select switch to *EP scale*. Read and record (2 scales).	
30	Remove Cs-137 and install Po-210. Mark H.P. (DAS) tape when change is made.	
	COSMIC DUST DETECTOR	

Step	Operation	Normal Indication
31	Excite earth actuator manually with one low pulse. Readout at DAS tape S/F 3 word 9 should read 001. Mark on DAS tape. Record data.	
32	Excite earth actuator manually with four low pulses. Readout should be 003. Mark on DAS tape. Record.	
33	Excite earth actuator manually with two high pulses. Readout should be 007. Mark DAS readout tape and record.	
34	Excite lunar actuator manually with one low pulse. Readout at DAS tape S/F 3 word 9 should read 010. Mark on DAS tape. Record data.	
35	Excite lunar actuator manually with four low pulses. Readout should be 030. Mark on DAS tape and record.	
36	Excite lunar actuator manually with two high pulses. Readout should be 010. Mark DAS readout tape and record.	
	LOW-ENERGY SOLAR PLASMA	
37	Set analog select switch to *LEP 1*. Verify experiment input switch set to open. Note master frame count. Read and record.	
38	Set experiment input switch to 0 v. Note M/F count. Read and record DAS readout tape. Make sure at least 10 M/F are run in this operating mode.	
39	Set experiment input switch to 1 v. Note M/F count. Read and record DAS readout tape. Allow to operate in this mode for 10 master frames.	
40	Set experiment input switch to 2 v. Note master frame count. Press DVM *read* during S/F 4 and 5. Mark DAS readout and DVM readout tapes. Record both readings. (LESP "A" is S/F 0, 1, 2, and 3, word 4)	
41	Set analog select switch to *LEP 2*. Input switch remains at 2 v. Note master frames count. Press DVM *read* during S/F 4 and 5. Mark DAS and DVM readout tapes. Record both readings. (*LEP 2* is S/F 0, 1, 2, and 3 word 8.)	
42	Set analog select switch to *LEP 3*. Input switch remains at 2 v. Press DVM *read* during S/F 4 and 5. Mark DAS and DVM readout tapes. Record. (*LEP 3* is S/F 0, 1, 2, and 3 word 12.)	
43	Set analog select switch to *LEP 4*. Input switch remains at 2 v. Press DVM *read* during S/F 4 and 5. Mark DAS and DVM readout tapes. Record. (*LEP 4* is S/F 0, 1, 2, and 3 word 16.)	
44	Set analog select switch to H.V. ana. (*LEP scale*). Input switch remains at 2 v. Press DVM *read* during S/F 4 and 5. Mark DAS and DVM readout tapes. Record. (*LEP scale* is S/F 0, 1, 2, 3, word 20.)	
45	After seeing that at least 10 master frames have passed since step 40, set *binary lock on*. Note on H.P. 562 tape.	
46	Set analog select switch to + *analyzer*. Press DVM *read*. Mark DAS and DVM readout.	
47	Set analog select switch to − *analyzer*. Press DVM *read*. Mark DAS and DVM readout.	
48	Set analog select switch to *deflection H.V.* Press DVM *read*. Mark DAS and DVM readout.	
49	Press *external binary drive* once. Mark DAS tape.	
50	Press DVM *read* to readout deflection H.V. a second time.	1. −1.5 to −7 v. 2. −0.5 to 0 v.
51	Set *binary lock off*. Mark DAS 562 tape.	
52	Turn experiment input switch to *off*.	
	SEARCH COIL MAGNETOMETER	
53	See that shorting plug is removed.	
54	After master frame count has passed XX7, press DVM *read* at S/F 3, 4, and 5. Mark and record DAS and DVM readout tapes. Allow magnetometer to operate in this mode until next M/F count XX7.	
55	At following M/F count of XX7, hold *IFC relay actuate* switch in and press *IFC on* switch. Record on DAS and DVM tapes. Press DVM *read* switch during next S/F 3, 4, and 5. (Analog select switch still at *300 cps.*) Mark and record DAS and DVM readout tapes.	END OF TEST

Table A-1. Voltage scanner format

Position	Experiment	Voltage	Tolerance, v
1	Particle flux	+6.5	±1
2	Particle flux	+16	±2
3	Electron flux	+7.2	±0.5
4	Electron flux	−7.2	±0.5
5	Electron flux	+2.4	±0.5
6	Electron flux	+14.5	±1
7	Cosmic dust	+3	±0.5
8	Cosmic dust	+3	±0.5
9	DAS	+6	±0.5
10	DAS	−6	±0.5
11	DAS	+12	±0.5
12	Magnetometer	+20	±0.5
13	Low-energy ion	+12	±1
14	Low-energy ion	−45	±1
15	Electron-proton spectrometer	+16	±1
16	Electron-proton spectrometer	+16.95	±0.5
17	Electron-proton spectrometer	+28	±0.5
18	Low-energy plasma	+6	±0.6
19	Low-energy plasma	+6	±0.6
20	Low-energy plasma	−6	±0.6
21	Low-energy plasma	−6	±0.6
22	Low-energy plasma	+12	±1.2
23	Low-energy plasma	+12	±1.2
24	Isolation box	+12	±1
25	Isolation box	−12	±1
26	SDT	−15	±1
27	SDT	+10	±1
28	CRA	+6	±1
29	CRA	−7.5	±0.5
30	CRA	−18	±1
31	CRA	−11	±1
32	Science inverter	−9	±0.9
33	Science inverter	+31.5	±0.5
34	Electron-proton spectrometer	+16.00	±1
35	Cosmic dust actuator	+50	±10
36	CRA	+18	±1